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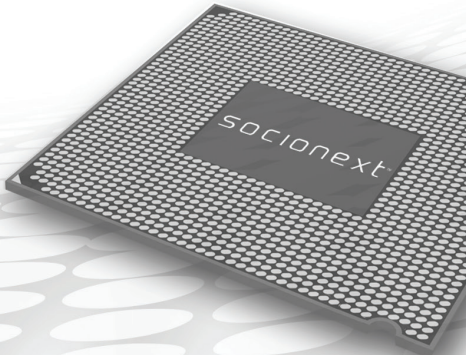
Corporate names revised in the documents

On March 1st 2015, system LSI businesses of Fujitsu Limited and Panasonic Corporation have been consolidated and transferred to Socionext Inc.

The corporate names “Fujitsu Semiconductor Limited” and “Panasonic” all in this document have been revised to the “Socionext”.

Thank you for your cooperation and understanding of this notice.

March 2, 2015
Socionext Inc.
http://www.socionext.com/en/



FUJITSU SEMICONDUCTOR
DATA SHEET

DS06–20210–4E

Semicustom

CMOS

Standard Cell

CS101 Series

■ DESCRIPTION

CS101 series, a 90 nm standard cell product, is a CMOS ASIC that satisfies user's demands for lower power consumption and higher speed. The leakage current of the transistors is the minimum level in the industry. Three types of core transistors with a different threshold voltage can be mixed according to user application.

The design rules match industry standards, and a wide range of IP macros are available for use.

As well as providing a maximum of 91 million gates, approximately twice the level of integration achieved in previous products, the power consumption per gate is also reduced by about half to 2.7 nW. Also, using the high-speed library increases the speed by a factor of approximately 1.3, with a gate delay time of 12 ps.

■ FEATURES

- Technology : 90 nm Si gate CMOS
  6- to 10-metal layers.
  Low-K (low permittivity) material is used for all dielectric inter-layers.
  Three different types of core transistors (low leak, standard, and high speed) can be used on the same chip.
  The design rules comply with industry standard processes.
- Power supply voltage : + 0.9 V to + 1.3 V (A wide range is supported.)
- Operation junction temperature : − 40 °C to + 125 °C (standard)
- Gate delay time : t_{pd} = 12 ps (1.2 V, Inverter, F/O = 1)
- Gate power consumption : 2.7 nW/gate (1.2 V, 2 NAND, F/O = 1, operating rate 0.5) ,
  1.8 nW/gate (1.0 V, 2 NAND, F/O = 1, operating rate 0.5)
- High level of integration : Up to 91 million gates
- Reduced chip sized realized by I/O with pad.
- Two types of library sets are supported. (Performance focused (1.2 V) , Low power consumption supported (0.9 V to 1.3 V))
- Low power consumption design (multi-power supply design and power gating) is supported.
- Compliance with industry standard design rules enables non-Fujitsu Semiconductor commercial macros to be easily incorporated.
- Compiled cell (RAM, ROM, others)
- Support for ultra high speed (up to 10 Gbps) interface macros.
- Special interfaces (LVDS, SSTL2, others)
- Supports use of industry standard libraries (.LIB).
- Uses industry standard tools and supports the optimum tools for the application.

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- Short-term development using a physical prototyping tool
- One pass design using a physical synthesis tool
- Hierarchical design environment for supporting large-scale circuits
- Support for Signal Integrity, EMI noise reduction
- Support for static timing sign-off
- Optimum package range : FBGA, FC-BGA, PBGA,TEBGA

■ MACRO LIBRARIES

1. Logic cells (about 400 types)

Unit cell having three different types of core transistors with a different threshold value are provided.

- Adder
- AND
- AND-OR
- AND-OR Inverter
- Buffer
- Clock Buffer
- Delay Buffer
- ENOR
- EOR
- Inverter
- Latch
- NAND
- NOR
- OR
- OR-AND
- OR-AND Inverter
- SCAN Flip flop
- Non-SCAN Flip Flop
- Selector
- Others

2. IP macros

Compliance with the design rules recommended by the industry standard STARC (Semiconductor Technology Academic Research Center) recommendations which means a wide range of commercially available IP macros can be used.

CPU/DSP	ARM™* core (ARM7TDMI-S™*, ARM946E-S™*, ARM1176JZF-S™*), FR71E core
Mixed signal macro	ADC, DAC, OPAMP, others
Compiled macro	RAM (1-port, 2-port), ROM, product sum calculator, others
PLL	Analog PLL

*: ARM, ARM7TDMI-S, ARM946E-S and ARM1176JZF-S are the trademarks of ARM Limited in the EU and other countries.

3. Special I/O interface macro

Interface macro (PHY)	LVDS, SSTL2, SSTL18, PCI, I^2C
Interface macro (Controller)	USB2.0 Device/host, Serial ATA, PCI-Express, DDR2, HDMI, others

■ COMPILED CELL

Compiled cells are macro cells which are automatically generated with the bit/word configuration specified. The CS101 series has the following types of compiled cells. (Note that each macro is different in word/bit range depending on the column type.)

1. Clock synchronous single-port RAM (1 address : 1 read/write)

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
4	16 to 288 K	16 to 2 K	1 to 144
8	32 to 576 K	32 to 8 K	1 to 72
16	64 to 576 K	64 to 16 K	1 to 36

2. Clock synchronous dual port RAM (2 address : 2 read/write)

Column type (bit)	Memory capacity (bit)	Word range (word)	Bit range (bit)
4	16 to 144 K	8 to 1 K	2 to 144
8	64 to 288 K	32 to 4 K	1 to 72
16	64 to 144 K	32 to 4 K	2 to 36

3. Clock synchronous ROM

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
16	256 to 4 M	128 to 16 K	2 to 256
64	1 K to 4 M	512 to 64 K	2 to 64

4. Clock synchronous register file (2 address : 1 read, 1 write)

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
1	8 to 18 K	4 to 128	2 to 144

5. Clock synchronous register file (4 address : 2 read, 2 write)

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
1	8 to 18 K	4 to 128	2 to 144

6. Clock synchronous dual port RAM (2 address : 1 read, 1 write)

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
2	64 to 72 K	32 to 512	2 to 144
4	128 to 72 K	64 to 1 K	2 to 72
8	256 to 72 K	128 to 2 K	2 to 36

■ LARGE CAPACITY MEMORY

Clock synchronous single-port RAM (1 address : 1 read/write)

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
16	64 K to 9 M	8 K to 64 K	8 to 144

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Application	Rating		Unit
			Min	Max	
Power supply voltage*1	V_{DD}	V_{DDI} (Internal)	− 0.5	+ 1.8	V
		V_{DDE} (External 1.8 V)	− 0.5	+ 2.5	V
		V_{DDE} (External 2.5 V)	− 0.5	+ 3.6	V
		V_{DDE} (External 3.3 V)	− 0.5	+ 4.6	V
Input voltage *1,*2	VI	1.8 V	− 0.5	V_{DDE} + 0.5 (≤ 2.5)	V
		2.5 V	− 0.5	V_{DDE} + 0.5 (≤ 3.6)	V
		3.3 V	− 0.5	V_{DDE} + 0.5 (≤ 4.6)	V
Output voltage*1	VO	1.8 V	− 0.5	V_{DDE} + 0.5 (≤ 2.5)	V
		2.5 V	− 0.5	V_{DDE} + 0.5 (≤ 3.6)	V
		3.3 V	− 0.5	V_{DDE} + 0.5 (≤ 4.6)	V
Storage temperature	T_{STG}	Plastic package	− 55	+ 125	°C
Operation junction temperature	Tj	—	− 40	+ 125	°C
Power supply pin current *3	ID	per V_{DDI}, V_{DDE} V_{SS} pin	—	*5	mA
Output current *4	IO	—	—	*5	mA

*1 : V_{SS} = 0 V

*2 : The values vary depending on the type of macros.

*3 : Maximum power supply current that can steadily flow.

*4 : Maximum output current that can steadily flow.

*5 : Contact the sales representative for details.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

• Dual power supply (V_{DDE} = 1.8 V ± 0.15 V , V_{DDI} = 1.0 V ± 0.1 V/V_{DDI} = 1.2 V ± 0.1 V)

(V_{SS} = 0 V)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply voltage		V_{DDE}	1.65	1.8	1.95	V
		V_{DDI}	0.9	1.0	1.1	V
			1.1	1.2	1.3	
“H” level input voltage	1.8 V CMOS Normal	V_{IH}	$V_{DDE} \times 0.65$	—	V_{DDE}+0.3	V
	1.8 V CMOS Schmitt		$V_{DDE} \times 0.70$	—	V_{DDE} + 0.3	V
“L” level input voltage	1.8 V CMOS Normal	V_{IL}	–0.3	—	$V_{DDE} \times 0.35$	V
	1.8 V CMOS Schmitt		–0.3	—	$V_{DDE} \times 0.30$	V
Schmitt hysteresis voltage		VH	$V_{DDE} \times 0.10$	—	$V_{DDE} \times 0.40$	V
Operation junction temperature		Tj	–40	—	+125	°C

• Dual power supply (V_{DDE} = 2.5 V ± 0.2 V , V_{DDI} = 1.0 V ± 0.1 V/V_{DDI} = 1.2 V ± 0.1 V)

(V_{SS} = 0 V)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply voltage		V_{DDE}	2.3	2.5	2.7	V
		V_{DDI}	0.9	1.0	1.1	V
			1.1	1.2	1.3	
“H” level input voltage	2.5 V CMOS Normal	V_{IH}	1.7	—	V_{DDE} + 0.3	V
	2.5 V CMOS Schmitt		1.7	—	V_{DDE} + 0.3	V
“L” level input voltage	2.5 V CMOS Normal	V_{IL}	–0.3	—	+ 0.7	V
	2.5 V CMOS Schmitt		–0.3	—	+ 0.7	V
Schmitt hysteresis voltage		VH	0.2	—	1.0	V
Operation junction temperature		Tj	–40	—	+125	°C

• Dual power supply (V_{DDE} = 3.3 V ± 0.3 V , V_{DDI} = 1.0 V ± 0.1 V/V_{DDI} = 1.2 V ± 0.1 V)

(V_{SS} = 0 V)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply voltage		V_{DDE}	3.0	3.3	3.6	V
		V_{DDI}	0.9	1.0	1.1	V
			1.1	1.2	1.3	
“H” level input voltage	3.3 V CMOS Normal	V_{IH}	2.0	—	V_{DDE} + 0.3	V
	3.3 V CMOS Schmitt		2.1	—	V_{DDE} + 0.3	V
“L” level input voltage	3.3 V CMOS Normal	V_{IL}	–0.3	—	+ 0.8	V
	3.3 V CMOS Schmitt		–0.3	—	+ 0.7	V
Schmitt hysteresis voltage		VH	0.2	—	1.4	V
Operation junction temperature		Tj	–40	—	+125	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

• Dual power supply : V_{DDE} = 1.8 V, V_{DDI} = 1.0 V/V_{DDI} = 1.2 V
(V_{DDE} = 1.8 V ± 0.15 V, V_{DDI} = 1.0 V ± 0.1 V/V_{DDI} = 1.2 V ± 0.1 V, V_{SS} = 0 V, Tj = –40 °C to +125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
"H" level output voltage	V_{OH}	1.8 V output, I_{OH} = –100 µA	V_{DDE} – 0.2	—	V_{DDE}	V
"L" level output voltage	V_{OL}	1.8 V output, I_{OL} = 100 µA	0	—	0.2	V
Input leakage current*	IL	VI = 0 V or VI = V_{DDE}	– 10	—	+ 10	µA
Pull-up/Pull-down resistor	Rp	1.8 V V_{IL} = 0 V at pull-up/ V_{IH} = V_{DDE} at pull-down	40	80	155	kΩ

* : The input leakage current may exceed the above value when an input buffer with pull-up or pull-down resistor is used.

• Dual power supply : V_{DDE} = 2.5 V, V_{DDI} = 1.0 V/V_{DDI} = 1.2 V
(V_{DDE} = 2.5 V ± 0.2 V, V_{DDI} = 1.0 V ± 0.1 V/V_{DDI} = 1.2 V ± 0.1 V, V_{SS} = 0 V, Tj = –40 °C to +125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
"H" level output voltage	V_{OH}	2.5 V output, I_{OH} = –100 µA	V_{DDE} – 0.2	—	V_{DDE}	V
"L" level output voltage	V_{OL}	2.5 V output, I_{OL} = 100 µA	0	—	0.2	V
Input leakage current*	IL	VI = 0 V or VI = V_{DDE}	– 10	—	+ 10	µA
Pull-up/Pull-down resistor	Rp	2.5 V V_{IL} = 0 V at pull-up/ V_{IH} = V_{DDE} at pull-down	25	50	85	kΩ

* : The input leakage current may exceed the above value when an input buffer with pull-up or pull-down resistor is used.

• Dual power supply : V_{DDE} = 3.3 V, V_{DDI} = 1.0 V/V_{DDI} = 1.2 V
(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.0 V ± 0.1 V/V_{DDI} = 1.2 V ± 0.1 V, V_{SS} = 0 V, Tj = –40 °C to +125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
"H" level output voltage	V_{OH}	3.3 V output, I_{OH} = –100 µA	V_{DDE} – 0.2	—	V_{DDE}	V
"L" level output voltage	V_{OL}	3.3 V output, I_{OL} = 100 µA	0	—	0.2	V
Input leakage current*	IL	VI = 0 V or VI = V_{DDE}	–10	—	+ 10	µA
Pull-up/Pull-down resistor	Rp	3.3 V V_{IL} = 0 V at pull-up/ V_{IH} = V_{DDE} at pull-down	15	33	70	kΩ

* : The input leakage current may exceed the above value when an input buffer with pull-up or pull-down resistor is used.

■ AC CHARACTERISTICS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Delay time	t_{pd}*1	typ *2 × tmin *3	typ *2 × ttyp *3	typ *2 × tmax *3	ns

*1 : Delay time = propagation delay time, enable time, disable time

*2 : “typ” is calculated based on the cell specifications.

*3 : Measurement condition

Measurement condition	tmin	ttyp	tmax
V_{DD} = 1.2 V ± 0.1 V, V_{SS} = 0 V, Tj = – 40 °C to +125 °C	0.62	1.00	1.57

Note : The values are reference values, which vary depending on the cells.

■ I/O PIN CAPACITANCE

Parameter	Symbol	Value	Unit
Input pin	C_{IN}	Max16	pF
Output pin	C_{OUT}	Max16	pF
I/O pin	$C_{I/O}$	Max16	pF

Note : The capacitance values vary depending on the package and pin positions.

■ DESIGN METHODS

Fujitsu Semiconductor’s Reference Design Flow provides the following functions that help shorten the development time of large scale and high quality LSIs.

- High reliability design estimation in the early stage of physical design realized by physical prototyping.
- Layout synthesis with optimized timing realized by physical synthesis tools.
- High accuracy design environment considering drop in power supply voltage, signal noise, delay penalty, and crosstalk.
- I/O design environment (power line design, assignment and selection of I/Os, package selection) considering noise.

■ PACKAGES

Packages available for existing series can be used for CS101 series. This allows smooth replacement with previously developed products.

For details of delivery times, contact the sales representative.

FBGA package : Max 906 pins

FC-BGA package : Max 2116 pins

PBGA package : Max 1156 pins

TEBGA package : Max 1156 pins