socionext™
for better quality of experience

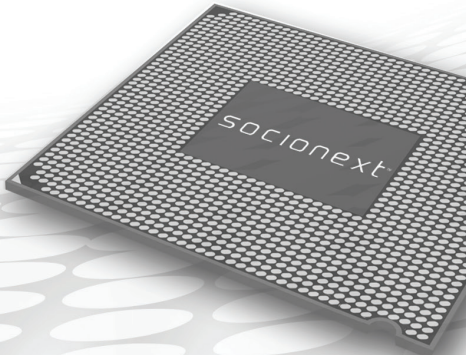
# Corporate names revised in the documents

On March 1st 2015, system LSI businesses of Fujitsu Limited and Panasonic Corporation have been consolidated and transferred to Socionext Inc.

The corporate names “Fujitsu Semiconductor Limited” and “Panasonic” all in this document have been revised to the “Socionext”.

Thank you for your cooperation and understanding of this notice.

March 2, 2015
Socionext Inc.
http://www.socionext.com/en/



FUJITSU SEMICONDUCTOR
DATA SHEET

DS06–20212–2E

*Semicustom*

**CMOS**

# Standard Cell

# CS302 Series

## ■ DESCRIPTION

The CS302 series of 40 nm standard cells is a line of CMOS ASICs that satisfy demands for lower power consumption, higher speed and higher integration.

These cells offer the minimum level of leakage current in the semiconductor industry, and are able to implement a mixture of core transistors with three different threshold voltages, as appropriate for the applications ranging from handheld terminals to digital audiovisual equipment.

The integration level in this series is twice the CS201 series with lower power consumption.

## ■ FEATURES

- Technology : 40 nm Si-gate CMOS
  : Maximum 11-metal layers. Extreme Low-K (ultra low permittivity) material is used for dielectric inter-layers.
  : Three different types of core transistors (low leak, standard and high speed) can be used on the same chip.
- Supply voltage : + 1.1 V ± 0.1 V
- Junction temperature range : – 40 °C to +125 °C
- Gate power consumption : 1.02 nW / gate (operating condition: 1.1 V, operating rate 0.5, 1 MHz)
- High-quality, various types of cell sets developed by FUJITSU SEMICONDUCTOR (from low power versions to high speed versions).
- It supports energy-saving mode, multi mode SRAM.
- Compiled cells (RAM, ROM, others)
- Support low-consumption technology
- Support ultra high speed (up to 10 Gbps) interface macros
- Special interfaces (LVDS, SSTL, others)
- Supports boundary SCAN test
- Supports use of industry standard libraries
- Supports use of industry standard tools.
- Short-term development using a physical prototyping tool.
- One pass design using a physical synthesis tools.
- Hierarchical design environment for supporting large-scale circuits.
- Supports Signal Integrity, EMI noise reduction
- Supports static timing sign-off
- Improve timing convergence by using Statistical Static Timing Analysis (SSTA).

*(Continued)*


2011.7

FUJITSU

*(Continued)*

- Design For Manufacturing (DFM) enables stable product-supply and reduced variation
- Package lineup: FBGA, PBGA, TEBGA, FC-BGA

Note: Including items under development.

## ■ MACRO LIBRARIES (INCLUDING MACROS CURRENTLY BEING PREPARED)

### 1. Logic cells (about 400 types)

Library sets having three different threshold voltages of core transistors.

- Adder
- And
- AND-OR
- AND-OR Inverter
- Buffer
- Clock-Buffer
- Delay Buffer
- ENOR
- EOR
- Inverter
- Latch
- NAND
- NOR
- OR
- OR-AND
- OR-AND Inverter
- SCAN Flip flop
- Non-SCAN Flip flop
- Selector
- Others

### 2. IP macros

| | |
|---|---|
| CPU/DSP | ARM™* cores (ARM7TDMI-S™*, ARM946E-S™*, ARM926EJ-S™*, ARM1176JZF-S™*, Cortex™*-M3), Peripherals IP |
| Mixed signal macro | ADC, DAC,OPAMP, others. |
| Compiled macro | SRAM (1 Port,2 Port), 1 ROM, product sum calculator, others. |
| PLL | analog PLL |

*: ARM, ARM7TDMI-S, ARM946E-S, ARM926EJ-S, ARM1176JZF-S and Cortex are the trademarks of ARM Limited in the EU and other countries.

### 3. Special I/O interface macro

| | |
|---|---|
| Special I/O | LVDS, SSTL18, PCI, $I^2C$ |
| Interface macro | USB2.0 Device/host, Serial-ATA, PCI-Express, DDR2. HDMI, others. |

## ■ COMPILED CELL

Compiled cells are macro cells that can be automatically generated by specifying the bit/word configuration. The following compiled cells are available for the CS302 series (Note that the bit/word ranges for each macro vary depending on the column type).

### 1. Clock synchronous single-port RAM (1 address : 1 read/write)

| Column type | Memory capacity (bit) | Word range (word) | Bit range (bit) |
|---|---|---|---|
| 4 | 1 K to 1152 K | 128 to 8 K | 8 to 144 |
| 8 | 1 K to 1152 K | 256 to 16 K | 4 to 72 |
| 16 | 1 K to 624 K | 512 to 16 K | 2 to 39 |

### 2. Clock synchronous dual port RAM (2 address : 2 read/write)

| Column type | Memory capacity (bit) | Word range (word) | Bit range (bit) |
|---|---|---|---|
| 4 | 32 to 288 K | 16 to 4 K | 2 to 72 |
| 8 | 64 to 288 K | 32 to 8 K | 2 to 36 |
| 16 | 128 to 288 K | 64 to 16 K | 2 to 18 |

### 3. Clock synchronous ROM

| Column type | Memory capacity (bit) | Word range (word) | Bit range (bit) |
|---|---|---|---|
| 8 | 64 to 576 K | 32 to 4 K | 2 to 144 |
| 16 | 128 to 576 K | 64 to 8 K | 2 to 72 |
| 32 | 256 to 576 K | 128 to 16 K | 2 to 36 |
| 64 | 512 to 576 K | 256 to 32 K | 2 to 18 |

### 4. Clock synchronous register file (2 address : 1 read, 1 write)

| Column type | Memory capacity (bit) | Word range (word) | Bit range (bit) |
|---|---|---|---|
| 2 | 16 to 72 K | 8 to 1 K | 2 to 72 |
| 4 | 32 to 72 K | 16 to 2 K | 2 to 36 |
| 8 | 64 to 72 K | 32 to 4 K | 2 to 18 |
| 16 | 128 to 72 K | 64 to 8 K | 2 to 9 |

### 5. Clock synchronous register file (2 address : 2 read, 2 write)

| Column type | Memory capacity (bit) | Word range (word) | Bit range (bit) |
|---|---|---|---|
| 2 | 16 to 2.25 K | 8 to 16 | 2 to 144 |
| 4 | 64 to 18 K | 32 to 128 | 2 to 144 |

## ■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage*1 | $V_{DD}$ | − 0.4 | + 1.5 | V | *2 |
| | | − 0.5 | + 4.6 | | *3, *4 |
| Input voltage*1 | VI | − 0.5 | $V_{DD}$ + 0.5 ( ≤ 4.6 V) | V | *3, *4 |
| Output voltage*1 | VO | − 0.5 | $V_{DD}$ + 0.5 ( ≤ 4.6 V) | V | *3, *4 |
| Storage temperature | $T_{STG}$ | − 55 | + 125 | °C | |
| Operation junction temperature | Tj | − 40 | + 125 | °C | |
| Output current*5 | IO | — | — | mA | |
| Power supply pin current*6 | ID | — | — | mA | |

*1: $V_{SS}$ = 0 V.

*2: Internal gates

*3: 3.3 V interface on dual-power supply system

*4: For details about the power supply voltage, the input voltage and the output voltage for 1.8 V I/F and 2.5 V I/F, contact the sales representative.

*5: The output current varies depending on the number of wiring layers in the chip and the wiring configuration of the I/O cells. Contact the sales representative for details.

*6: The power supply pin current depends on the type of chip frame. Contact the sales representative for details.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

• **Dual power supply ($V_{DDE}$ = 3.3 V ± 0.3 V, $V_{DDI}$ = 1.1 V ± 0.1 V, $V_{SS}$ = 0 V)**

| Parameter | | Symbol | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Power supply voltage | | $V_{DDE}$ | 3.0 | 3.3 | 3.6 | V |
| | | $V_{DDI}$ | 1.0 | 1.1 | 1.2 | V |
| "H" level input voltage | 3.3 V CMOS | $V_{IH}$ | 2.0 | — | $V_{DDE}$ + 0.3 | V |
| "L" level input voltage | 3.3 V CMOS | $V_{IL}$ | − 0.3 | — | + 0.8 | V |
| Schmitt hysteresis voltage | | VH | 0.31 | 0.56 | 0.76 | V |
| Operation junction temperature | | Tj | − 40 | — | + 125 | °C |

• **Recommended Operating Conditions (Dual power supply: $V_{DDE}$ = 1.8 V, $V_{DDI}$ = 1.1 V)**

Contact the sales representative for details.

• **Recommended Operating Conditions (Dual power supply: $V_{DDE}$ = 2.5 V, $V_{DDI}$ = 1.1 V)**

Contact the sales representative for details.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

- **DC Characteristics (Dual power supply: $V_{DDE}$ = 3.3 V, $V_{DDI}$ = 1.1 V)**

  Measurement conditions: $V_{DDE}$ = 3.3 ± 0.3 V, $V_{DDI}$ = 1.1 V ± 0.1 V, $V_{SS}$ = 0 V, Tj = − 40 to + 125 °C

| Parameter | Symbol | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| "H" level input voltage | $V_{OH}$ | — | 2.4 | — | $V_{DDE}$ | V |
| "L" level input voltage | $V_{OL}$ | — | 0 | — | 0.4 | V |
| "H" level output current | $I_{OH}$ | 2 mA cell @$V_{OH}$ (Min) | − 13.2 | − 7.8 | − 3.9 | mA |
| | | 4 mA cell @$V_{OH}$ (Min) | − 26.3 | − 15.6 | − 7.9 | |
| | | 8 mA cell @$V_{OH}$ (Min) | − 52.7 | − 31.2 | − 15.8 | |
| | | 12 mA cell @$V_{OH}$ (Min) | − 79.0 | − 46.8 | − 23.7 | |
| | | 16 mA cell @$V_{OH}$ (Min) | − 105.1 | − 62.3 | − 31.5 | |
| | | 24 mA cell @$V_{OH}$ (Min) | − 140.0 | − 82.9 | − 42.0 | |
| "L" level output current | $I_{OL}$ | 2 mA cell @$V_{OL}$ (Max) | 2.2 | 3.5 | 4.8 | mA |
| | | 4 mA cell @$V_{OL}$ (Max) | 4.4 | 7.0 | 9.5 | |
| | | 8 mA cell @$V_{OL}$ (Max) | 8.9 | 13.9 | 19.1 | |
| | | 12 mA cell @$V_{OL}$ (Max) | 13.3 | 20.9 | 28.6 | |
| | | 16 mA cell @$V_{OL}$ (Max) | 17.8 | 27.9 | 38.1 | |
| | | 24 mA cell @$V_{OL}$ (Max) | 26.6 | 41.8 | 57.2 | |
| Input leakage current | IL | VI = 0 V or VI = $V_{DDE}$ | − 10 | — | + 10 | µA |
| Pull-up resistor | Rpu | VI = 0 V | 29 | 41 | 62 | kΩ |
| Pull-down resistor | Rpd | VI = $V_{DDE}$ | 30 | 44 | 72 | kΩ |

- **DC Characteristics (Dual power supply: $V_{DDE}$ = 1.8 V, $V_{DDI}$ = 1.1 V)**

  Contact the sales representative for details.

- **DC Characteristics (Dual power supply: $V_{DDE}$ = 2.5 V, $V_{DDI}$ = 1.1 V)**

  Contact the sales representative for details.

## ■ DESIGN METHODS

Fujitsu Semiconductor's Reference Design Flow provides the following functions that help reduce the development time of large scale, high quality LSIs.

- Statistical Static Timing Analysis (SSTA) improves timing convergence.
- Physical Prototyping enables more accurate estimation of highly reliable designs.
- Layout synthesis with optimized timing is realized by Physical Synthesis Tool.
- High accuracy design environment considers drop in power supply voltage, signal noise, delay penalty and crosstalk.
- I/O design environment (power line design, assignment and selection of I/Os, package selection) considers noise.

## ■ PACKAGES

The CS302 series can use the same packages that were available for the previous series, allowing a smooth transition from previously developed models. For details of delivery times, contact the sales representative.

- FBGA packages
- PBGA packages
- TEBGA packages
- FC-BGA packages