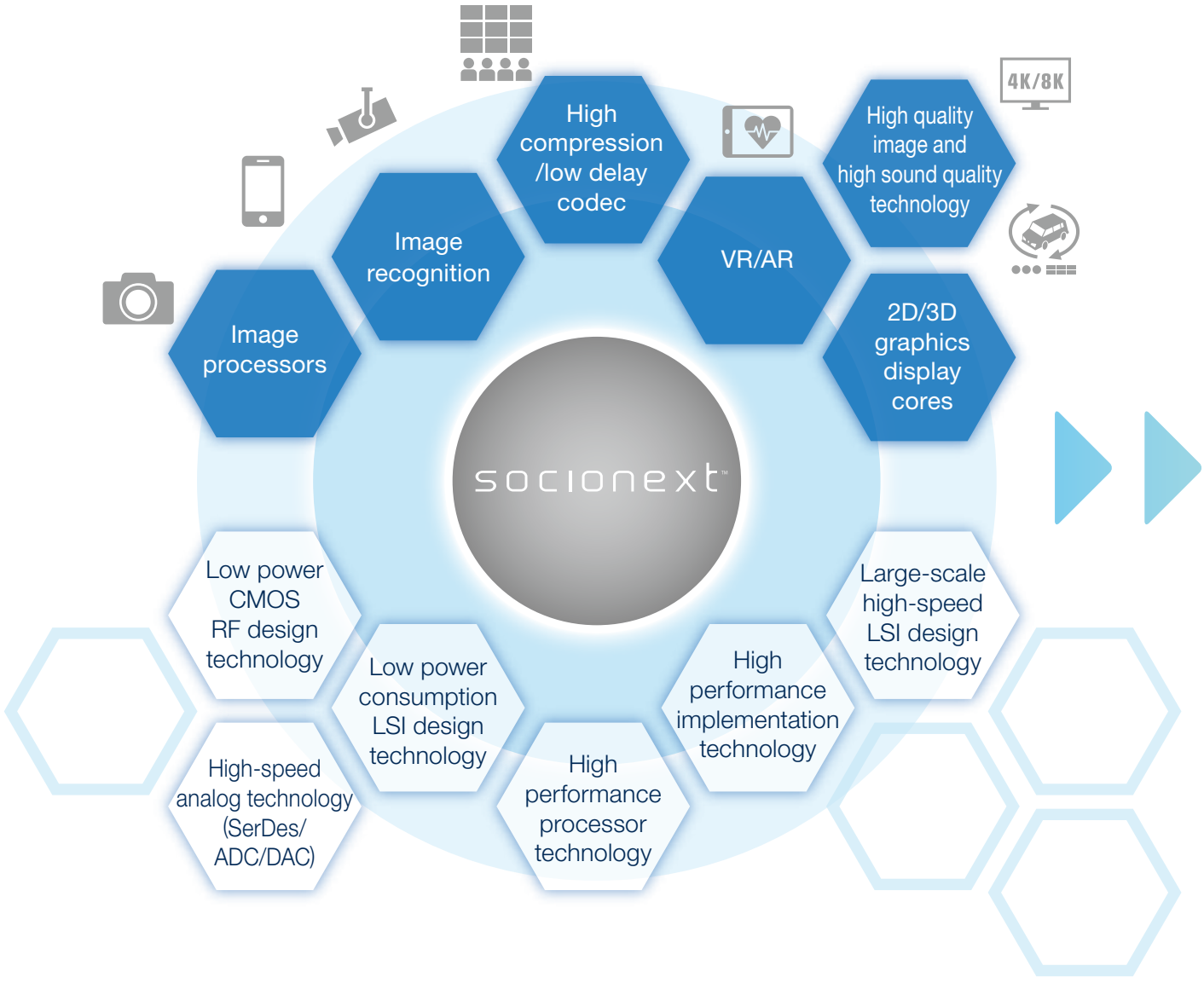
socionext™
for better quality of experience

Custom SoC(ASIC)

Custom SoC Solutions create New Value on your Next-Generation Products

With increasing functionality and higher performance of SoC, it is becoming more and more complicated to develop SoCs in a short time.
Over the past 40 years, Socionext's Custom SoC BU has earned reputation of being able to develop custom SoCs that meet our customers needs. Using our techniques of system architecture design, development support services, software platform, and customizing our ASSPs as core, we develop "One Step Ahead" system with you. We believe our role is to propose and provide custom SoC solutions that create new value in next generation products.

Socionext's ASSP Products/Core Technologies



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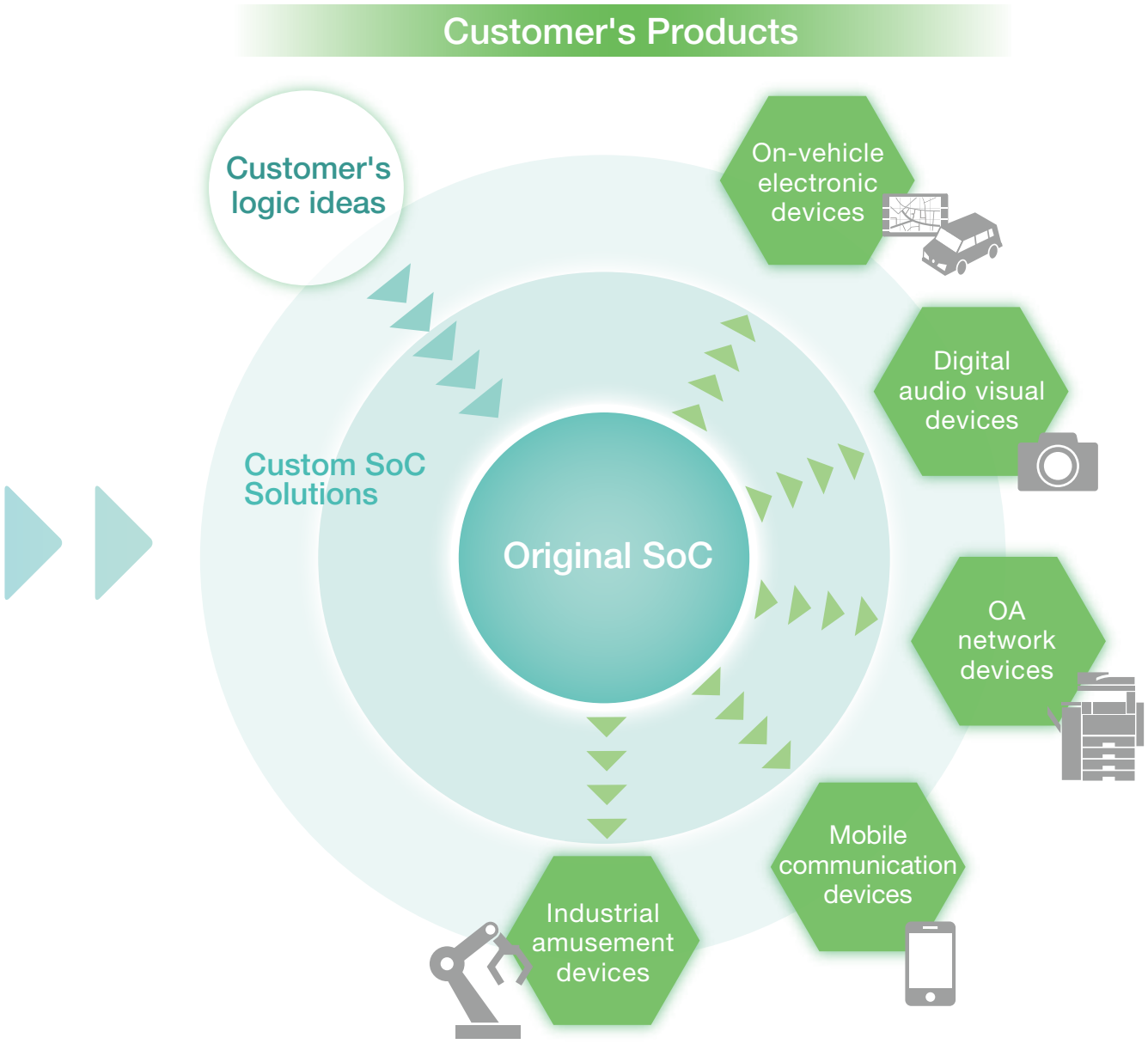
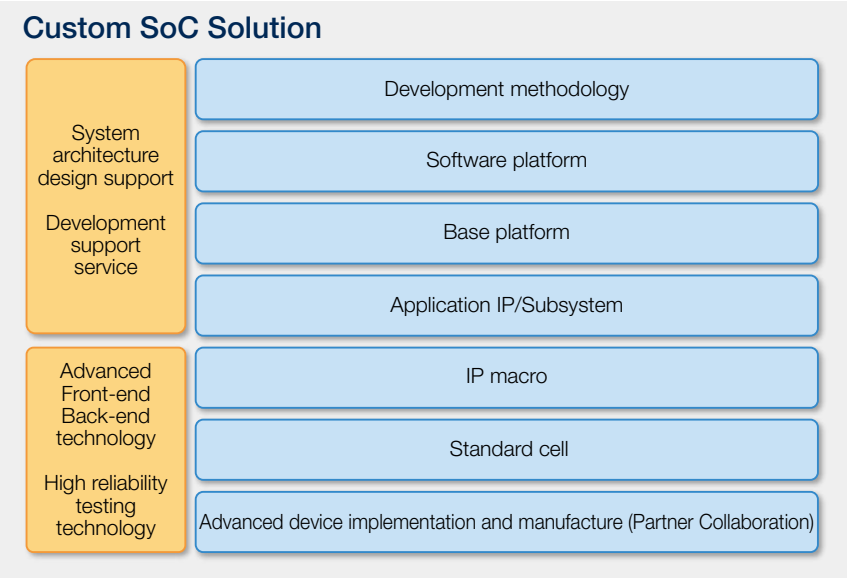


Custom SoC Solution

Custom SoC Solutions Overview

As for System on Chip (SoC) with CPU core, nowadays, various and highly functional SoCs development are demanded for a wide variation of CPU cores, high-performance buses, high-speed interfaces, and multi-functional IPs.

At the same time, for optimized customer's applications, it is becoming much complicated to select the best combination of components from the large number of combinations and it is becoming more harder to develop SoC in a short time. To deal with this situation, Socionext offers a "Custom SoC Solution" which integrates our development methodologies for ease of development, various platforms and development support services. Our "Custom SoC Solution" helps you to achieve high-perfomance and high-quality SoCs for your products in a short term.

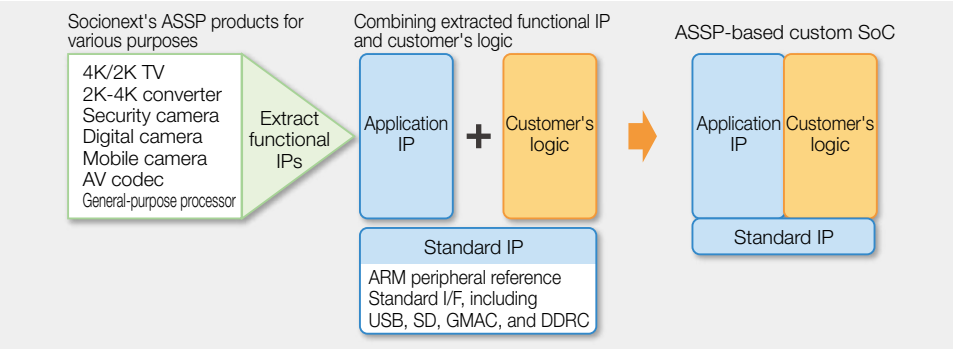


Development Methodology for Custom SoC Solutions

We provide four development methodology options for custom SoC solutions depending on the customer's application development period and budget.

ASSP-based Development

By customizing Socionext's ASSP (Application Specific Standard Procedure) products and combining with a variety of IPs, customer can reduce the development period for custom SoC and accelerate the product shipment.



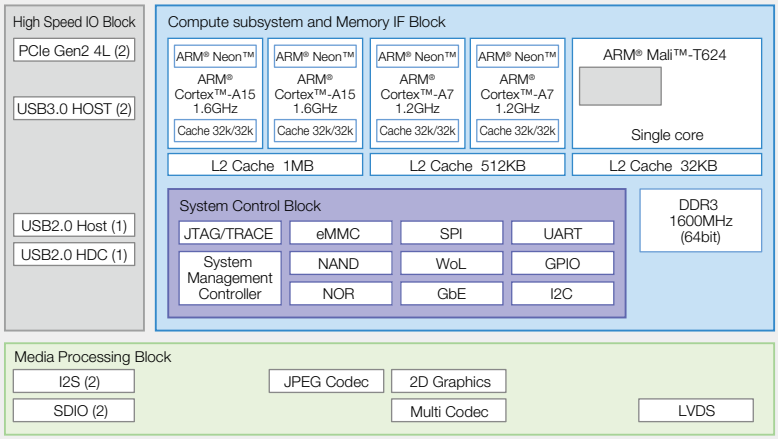
General-purpose Processor-based Development

We provide general-purpose processors for developing a high-performance, low power consumption system with high-performance CPUs and GPUs as well as high-speed interfaces at a low cost in a short time. We consider these general-purpose processors as a platform SoC.

Line-up of Platform SoC

	MB86S71	MB86S72	MB87S73
CPU	Cortex-A15 2core		-
	Cortex-A7 2core		
GPU	Mail-T624		
DDR	DDR3, DD3L, LPDDR3	DDR3, DD3L	
LAN	GbE, WoL TCP Accelaration		
FLASH	HSSPI, NOR, eMMC, NAND, HSSPI/NOR		
SERIAL	UART 3ch, GPIO 16ch, I2C 3ch	UART 3ch, GPIO 16ch, I2C 5ch	UART 3ch, GPIO 16ch, I2C 4ch
CODEC	4K multi-stream video, JPEG CODEC	JPEG CODEC	
DISPLAY	HDMI/MIPI DSI	FPD Link (4lane)	
AUDIO	2ch I2S		
SD	2ch SDIO		1ch SDIO
PCIe	1ch PCIe-Gen2-4lane	2ch PCIe-Gen2-4lane	
USB	USB 2.0, 3.0		

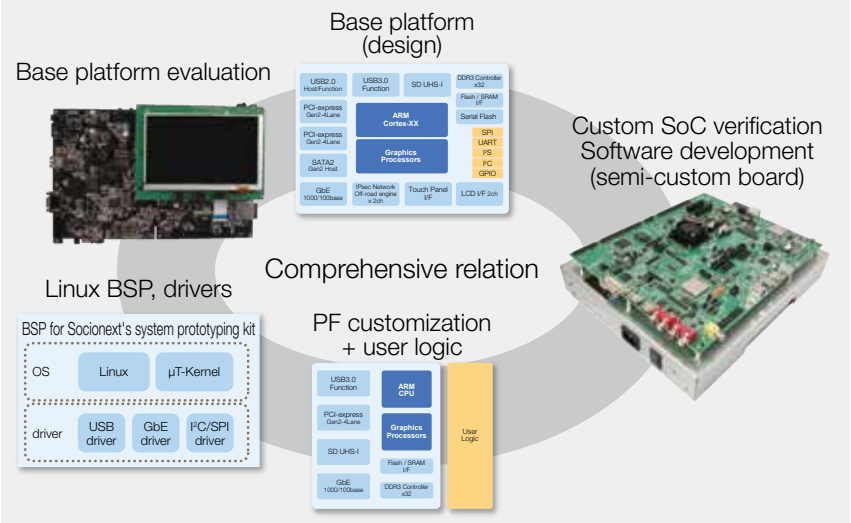
Platform SoC (MB86S72)



By combining customer's functional logic with our platform SoC, we reduce development risk of processor peripheral and high-speed I/Os and developing cost is also reduced significantly. It is also possible to integrate these system components into a single package with an optional SiP (system in a package) technology.

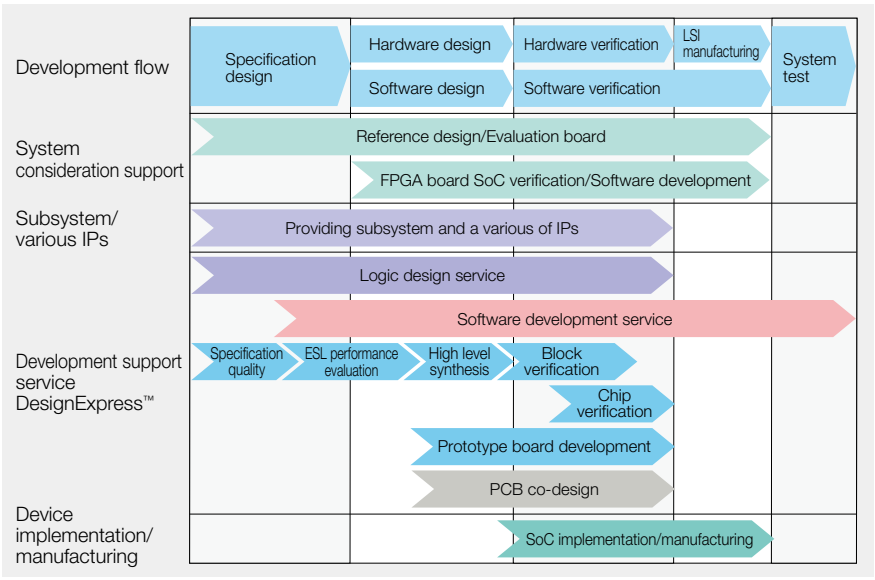
Platform-based Development

For your low risk development, we use platform SoC with a proven track record. After trimming unnecessary IPs and I/O's from our base platform SoC, we combine this trimmed parts and your customer's logic into a single chip.
You reduce re-make risk and development period significantly by 1. using our evaluation kit, 2. preliminary software development, 3. hardware development based on proved platform SoC, and 4. whole chip verification using semi-custom board.



Full Custom Development

To achieve the best performance of your SoC, we have full custom development option that allows you to customize as you like. For your full custom SoC development, we fully support for 1. proposing system architecture, 2. providing subsystem and a various of IPs, 3. optimized CPU peripheral design, and 4. system verification by hardware emulator and FPGA prototype. We also provide a device driver development service under contract as part of our software development support.

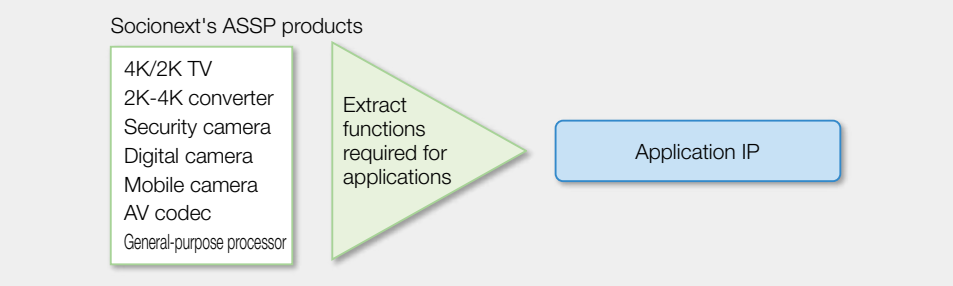


Example of ASSP-based Development

This section introduces one example of ASSP-based development.

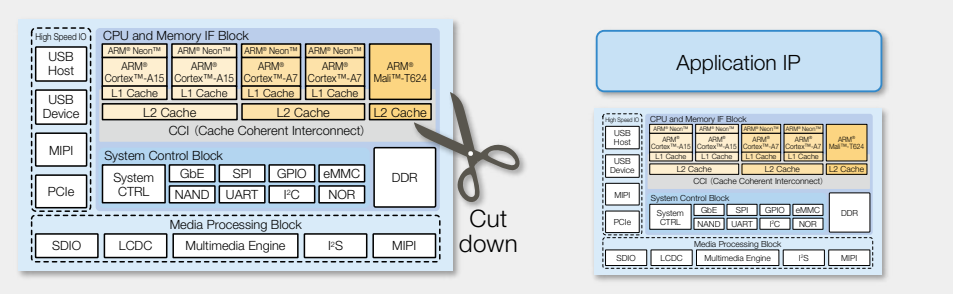
① Extracting necessary application IP from ASSP

We extract application IPs which are required for customer's development from our proven ASSP.



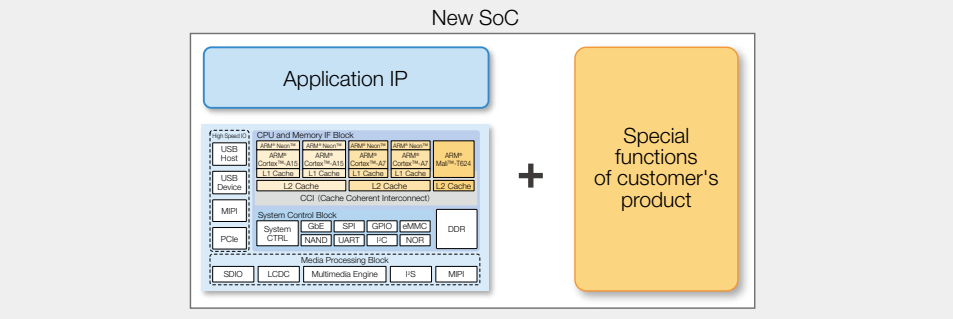
② Combining base platform and extracted application IP

After cutting down unnecessary IPs and Interfaces from base platform, then we combine this optimize platform and extracted application IP.



③ Adding your special functions to differentiate from others

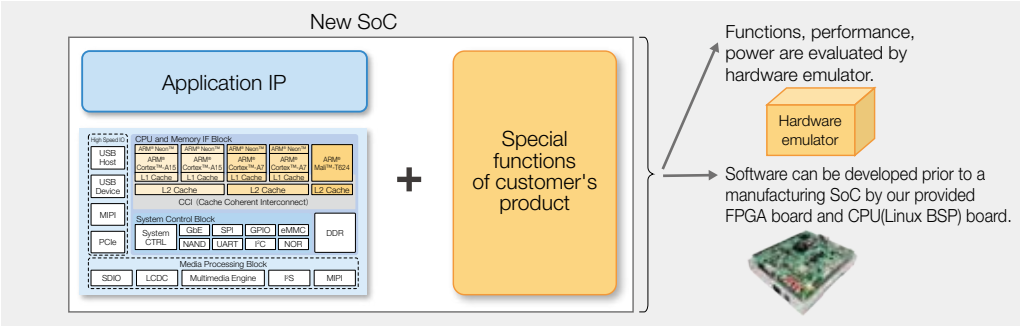
By adding your special functions to differentiate from others, your special SoC design is now created.



④ Evaluating and verifying functions, performance, and power

The functions, performance, and power can be evaluated and verified using a dedicated hardware emulator at approximately 1000 times as fast as an HDL simulator.

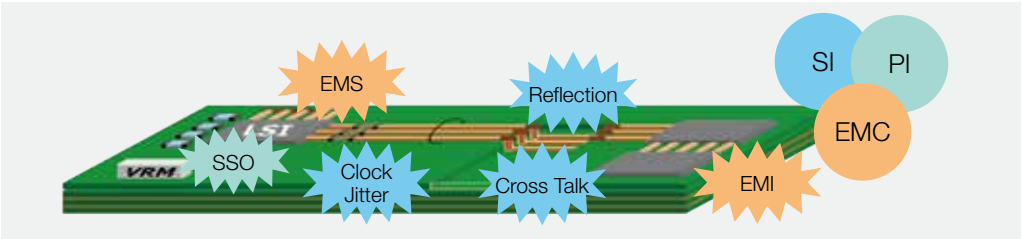
For your software development, we provide a prototype environment such as an FPGA board and CPU board. This allows customers to develop software before manufacturing SoC.



⑤ PCB (printed circuit board) co-design

Implementing high-speed components (DDR, PCIe, USB, etc.) and SoC on a PCB tends to cause a electrical issue such as electromagnetic noise, crosstalk, and clock jitter. We analyze such issue creating PCB prototype and offer proposed measures.

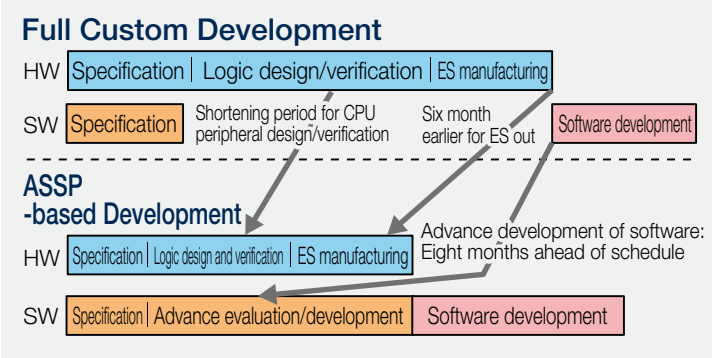
This reduces risk associated with developing a PCB and thereby reduces cost for PCB design and manufacturing.



Benefits of ASSP-based Development

From our experience of ASSP-based design for our product, the development period was achieved six months shorter than the development period by conventional design. This rapid time-to-market was achieved by shortening hardware design period and by developing software in advance.

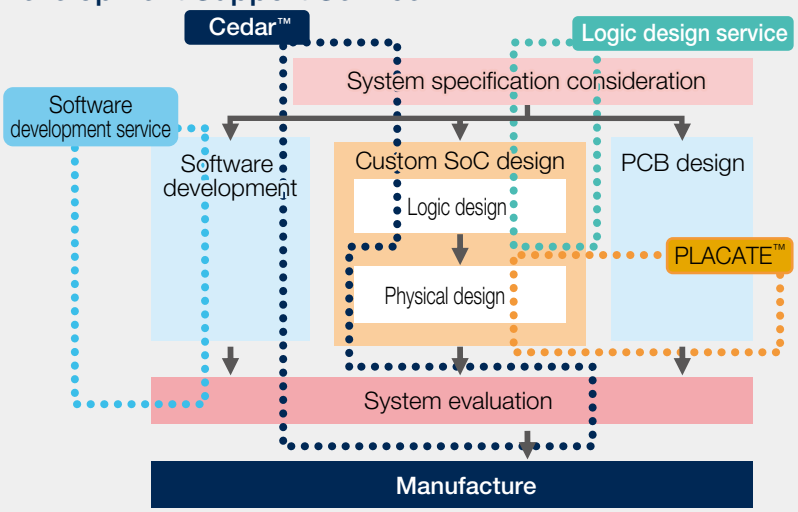
- Delivery time of sample SoC : Six months ahead of schedule
- Advance development of software : Eight months ahead of schedule
- Product shipping : Six months ahead of schedule



Development Support Service (DesignExpress™)

This design service provides consistent development support for everything from system specification to evaluation as well as for PCB design in custom SoC development for our customers. With this service, our customers can focus on differentiating their products while shortening the development period, reducing development risks, improving product quality, and reducing power consumption.

Relationship between Custom SoC Development Flow and Development Support Service



List of Development Support Services

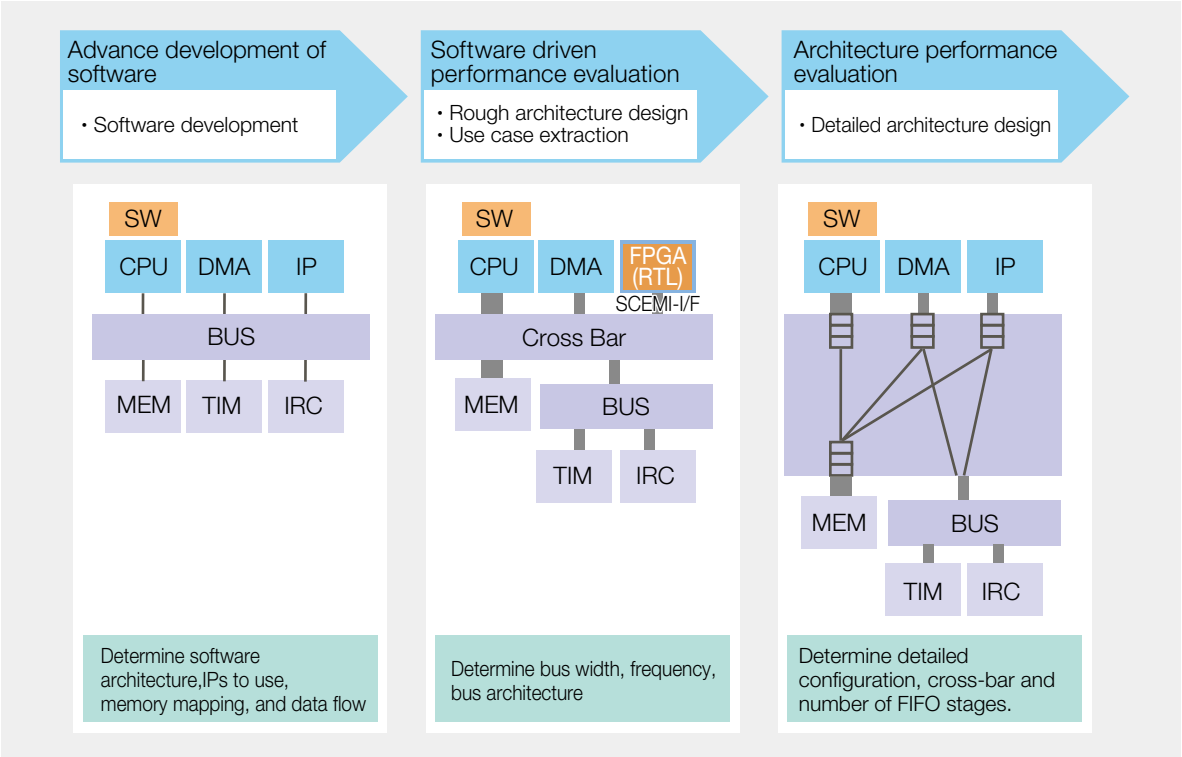
- Advance development of software and performance evaluation service in a virtual environment (Cedar™-ESL)
- High level synthesis support service (Cedar™-HLS)
- Logic design service
- Large-scale/long data verification and power consumption calculation service utilizing an emulator (Cedar™-EMU)
- Prototype board development service (Cedar™-PROT)
- PCB co-design support service (PLACATE™)
- Software development service
- Provide of subsystems

Advance development of software and performance evaluation service in a virtual environment (Cedar™-ESL)

Cedar™-ESL is used to develop software in advance using ESL technology (virtual platform) and also for software driven performance evaluation and architecture evaluation.
Software driven performance evaluation and architecture performance evaluation allow for architecture design to be performed at an early stage.

Example applications of Cedar™-ESL

- Division of functions between hardware and software enabled by advance development of software
- Architecture design and use case extraction based on software driven performance evaluation
- Detailed architecture design based on performance evaluation according to use cases



Service Category	Service Description	Item Submitted by Customer	Deliverable from Socionext (Example)
Provide of development environment for advance development of software	A virtual platform for software development is provided	Block diagram Block functional specification	High-speed virtual platform (for software development)
Provide of environment for software driven performance evaluation	A virtual platform for software driven performance evaluation is provided	Block diagram Block functional specification Software scenario	High-speed virtual platform (for architecture design)
Provide of environment for detailed architecture performance evaluation	A virtual platform for architecture performance evaluation is provided. Performance is measured	Architecture construction diagram Evaluation scenario	High-accuracy virtual platform Performance measurement report

High level synthesis Support service (Cedar™-HLS)

Cedar™-HLS is a service for mapping from a high-level language (C/SystemC) to our technology. This service reduces the cost and work period for our customers.

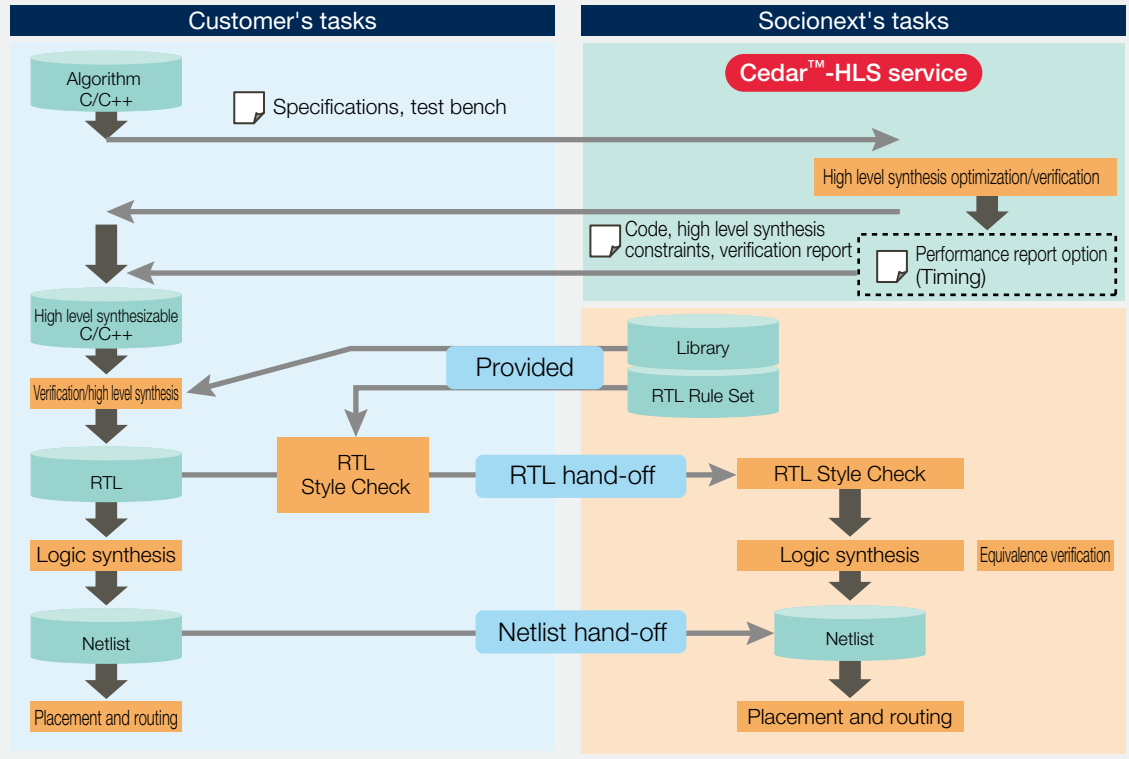
Benefits of high level synthesis

Reduced development period: the amount of description is reduced by one tenth and the verification time are reduced by one third (based on our results)
Reusing of sources: the efficiency of development can be improved (ease of changing devices/technologies)
Ease of evaluation: performance and footprint (cost) can easily be optimized using parameters

Example applications of Cedar™-HLS

Optimal source code tuning for custom SoCs (source code rewriting)
Confirmation of high level synthesis results and integrity by performing RTL logic synthesis

Cedar™-HLS Service Outline

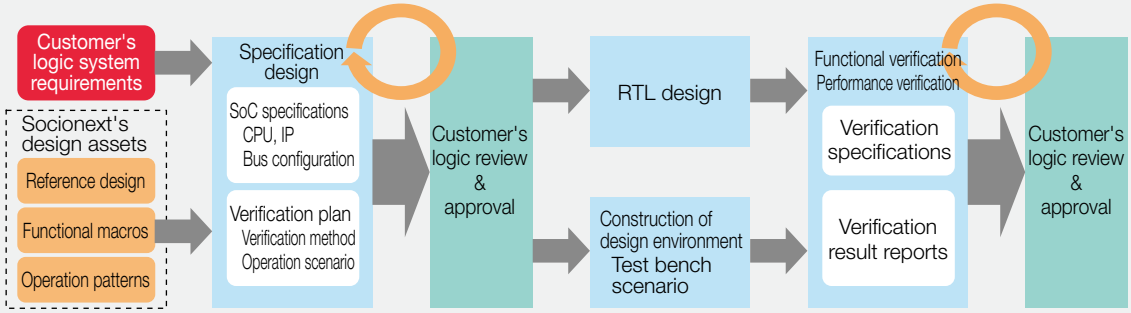


Service Category	Service Description	Item Submitted by Customer	Deliverable from Socionext (Example)
Handing off of RTL designed with high level synthesis RTL hand-off	Rewriting of a language in accordance with the tool Rewriting of a language in accordance with constraints	Functional specifications Constraint conditions High level language	Rewritten high level language Library for high level synthesis RTL designed with high level synthesis
Handing off of high level language	High level language is handed off and subsequent LSI design is performed under contract	(subject to the above described service)	SoC devices
Cedar™ coordination	High level synthesis of RTL for FPGA High level synthesis of RTL for ESL	Functional specifications Constraint conditions High level language	RTL SystemC

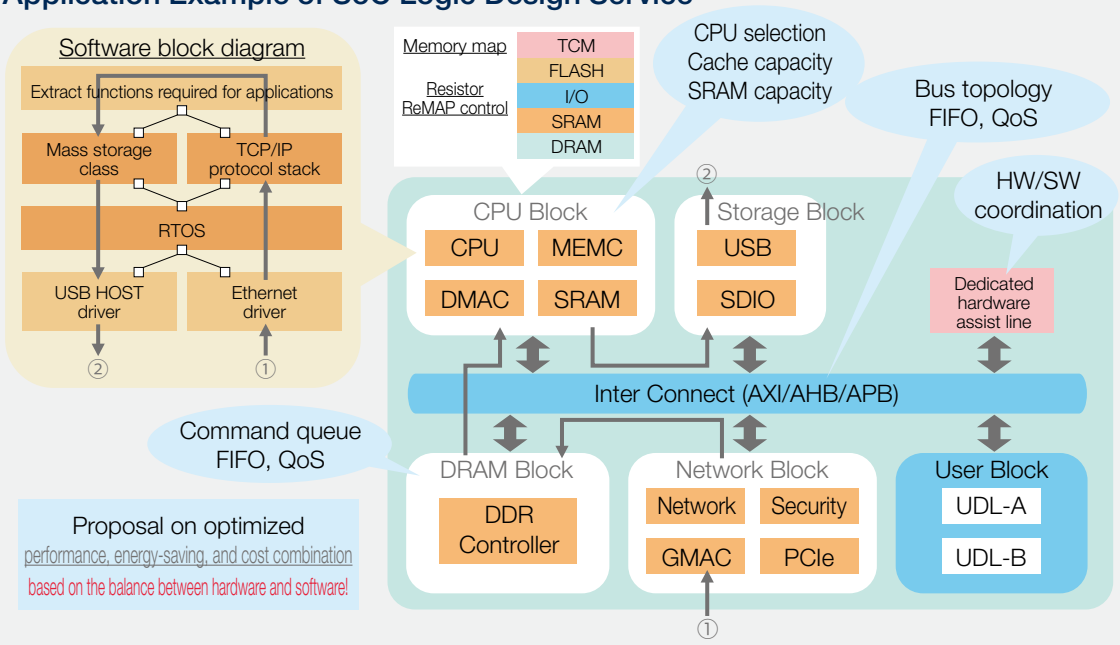
SoC Logic Design Service

By combining ARM's CPU and our various functional macros, we offer the best ARM platform for customers' systems. By suggesting a configuration of CPUs, buses, and memory controllers that takes performance and power into account and measuring performance at an early stage, we provide comprehensive support for custom SoC development. Customizing verified reference design (SNAP: Socionext ARM Based SoC Platform) allows us to provide high quality platforms in a short time.

SoC Logic Design Outline



Application Example of SoC Logic Design Service



Service Category	Service Description	Item Submitted by Customer	Deliverable from Socionext (Example)
SoC Logic Design	Specification design	Requirement specifications Macros to be installed Use cases Functional and performance requirements	SoC specifications
	RTL design		RTL
	RTL verification		Verification specifications,result reports

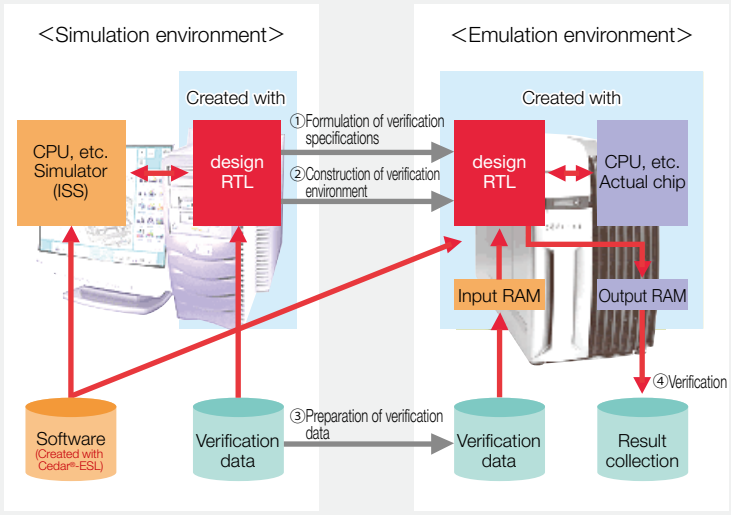
Large-scale/long data verification and power consumption calculation service utilizing an emulator (Cedar™-EMU)

This design service enables large-scale design to be verified by installing the design of a customer developing a custom SoC on an emulator and accelerating the HDL simulation time by 500 to 1000 times.
Since we provide the necessary equipment and operators, the customer only needs to prepare design data and input data to construct an environment.

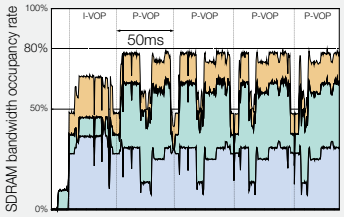
Example applications of Cedar™-EMU

- System verification of ARM-based image SoCs (ICE debugger can be connected)
- Simultaneous verification of hardware and software linked with ESL
- Functional and performance verification and power consumption analysis of image processing SoCs

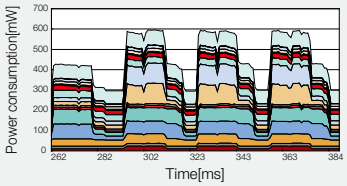
Cedar™-EMU Service Outline



Software debugging with ICE



Performance analysis with bus monitor



Power consumption analysis

We also develop technologies independently and have an option for various pre-silicon analysis.

- Software co-verification : Verification of a system including its software is possible in coordination with a Cedar™-ESL environment
- High accuracy performance display : Cycle accurate detailed performance analysis is possible
- High accuracy power consumption calculation : Power consumption is calculated with cell-level accuracy analysis is possible for each block

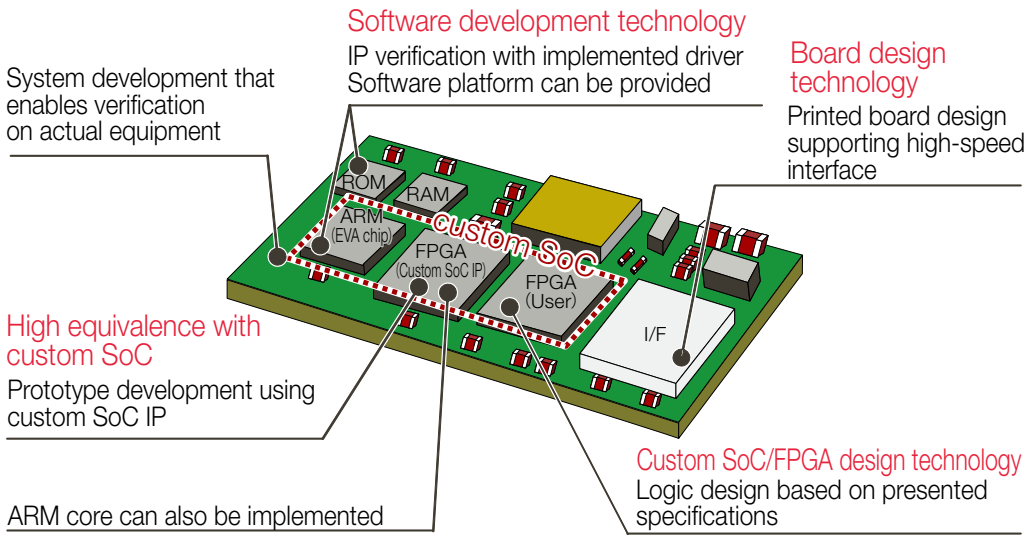
Service Category	Service Description	Item Submitted by Customer	Deliverable from Socionext (Example)
Chip level verification	Formulation of verification specifications Creation of verification data Construction of verification environment verification	Outline block diagram Design data (RTL or netlist) Input/expected value data	Verification specifications Verification data Emulation verification results
System level verification	System level verification using software developed in an ESL environment	Design data (RTL or netlist) Input/expected value data Test programs	Emulation verification environment Verification result reports
Power consumption reduction	Measurement of power consumption	Power measurement program	Reports on results of power consumption measurement

Prototype Board Development Service (Cedar™-PROT)

We provide a prototype board with an FPGA on which custom SoC design is implemented.
Since a custom SoC IP is implemented on an FPGA, high equivalence with the custom SoC can be maintained.
With the custom SoC IP and user logic implemented on separate FPGAs, this prototype board with a preverified IP allows customers to focus their efforts on the development of a user logic.

Example applications of Cedar™-PROT

- Prototype for system verification
- Prototype for advance development of software



Record of applications of Cedar™-PROT

- Controller custom SoC for network
- Custom SoC for measuring instruments
- Image processing custom SoC for documents
- Many others

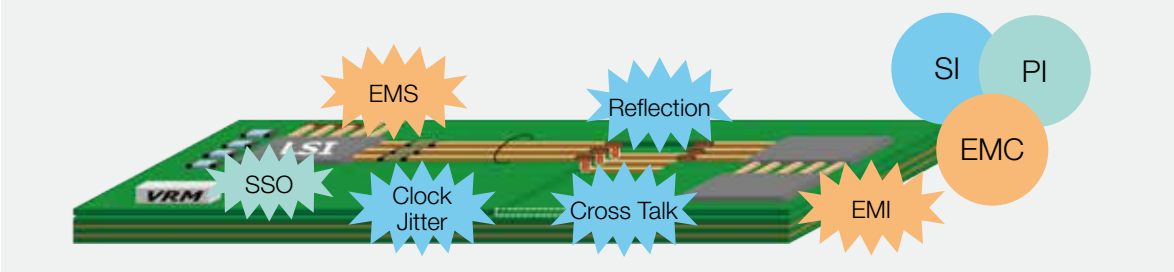
FPGA prototype board
Semi Custom board

FPGA prototype board for Cortex Mx

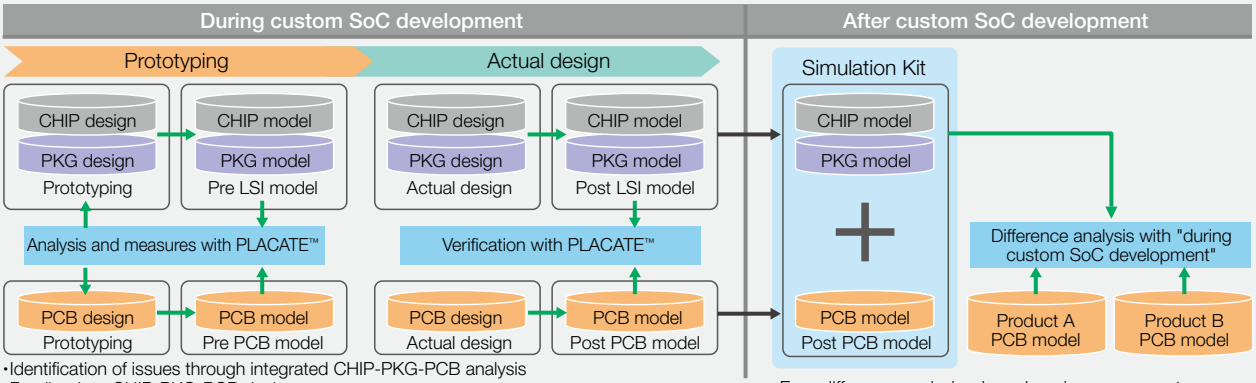
Service Category	Service Description	Item Submitted by Customer	Deliverable from Socionext (Example)
System level verification	Provide of a prototype board	Requirement specifications (specified circuit information,etc.)	Board unit Board specifications FPGA ROM data

PCB Co-design Support Service (PLACATE™)

PLACATE™ is a noise analysis and countermeasure support service based on an integrated LSI and PCB model that greatly supports customers in shortening the system development period and cost reductions through reduced BOM. By applying this service from the upstream phase of custom SoC design and PCB design, we contribute to shortening the design period of customers by reducing the amount of reworking of LSI and PCB design that needs to be done and thereby improving their systems and significantly reducing evaluation workload.

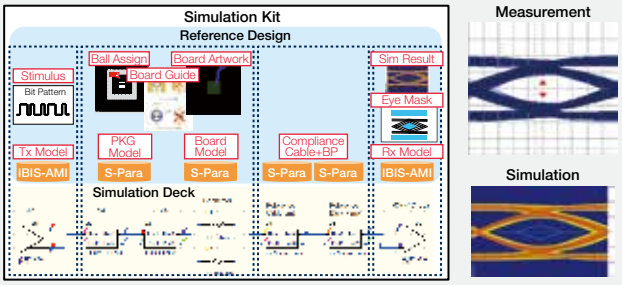


Design Flow Image

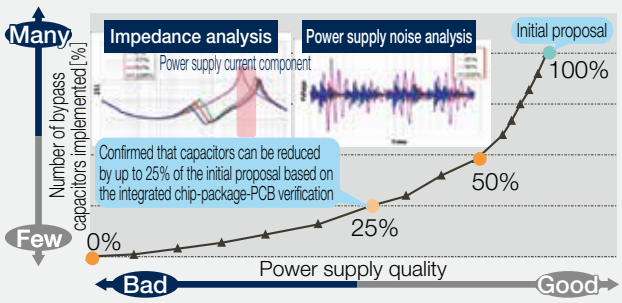


Service Description	Deliverable (Example)
■Board prototyping ・Wiring/Reducing bypass capacitors	Board design guidelines Board reference design
■Integrated noise analysis for LSI, PKG, and Board ・DRAM-IF (DDR4, etc.) SI/PI analysis ・SerDes (PCIe Gen3, etc.) SI analysis	SI/PI analysis result reports
■Creation of LSI power supply models ・LPM+IBIS5.0	LSI power supply model (LPM+ IBIS5.0)
■Looking into measures for EMC ・Consulting by iNARTE engineers	EMI analysis results EMI countermeasure proposals

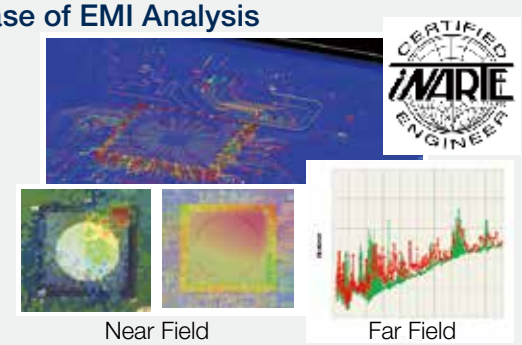
Structure of Simulation Kit



Case of Bypass Capacitor Reduction



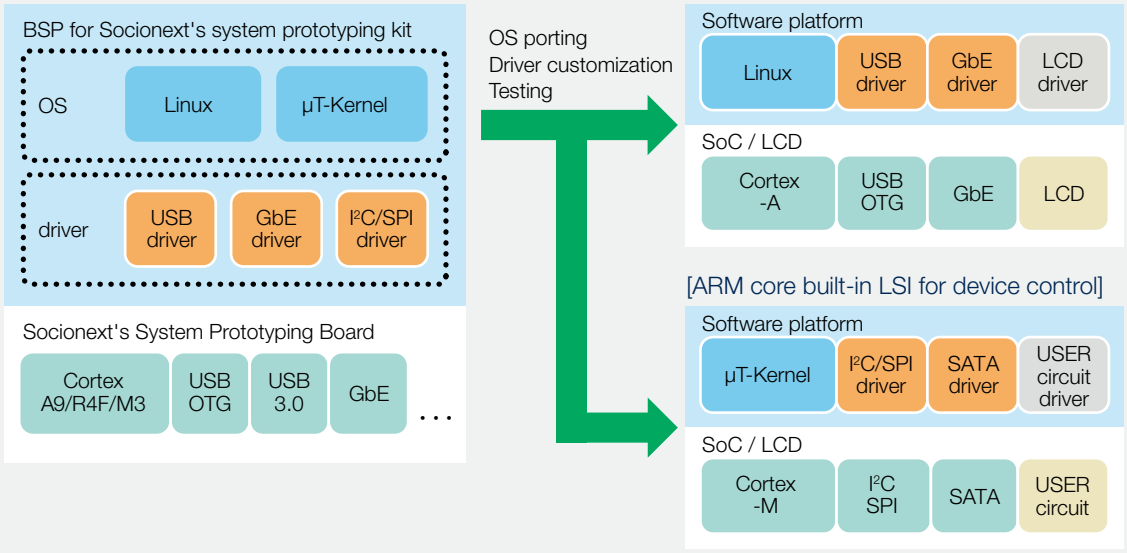
Case of EMI Analysis



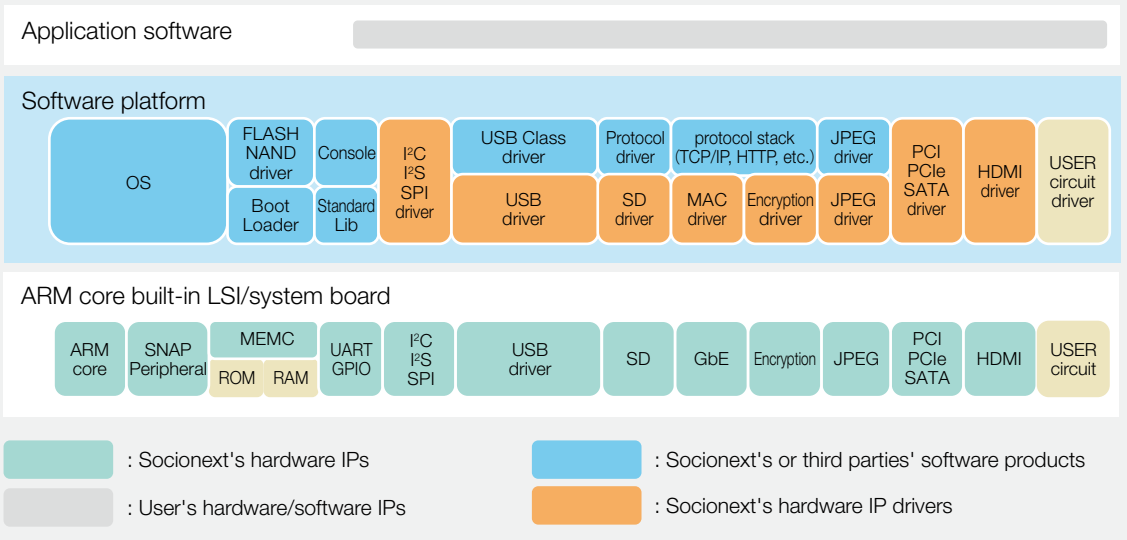
Software Development Service

This service provides a software platform customized for ARM-SoCs to be developed by customers, based on our system prototyping kit BSP (board support package).
Customers can focus their efforts on the development of application software without being bothered by the development of general-purpose functions and shorten the development period of products.

Example of Customization



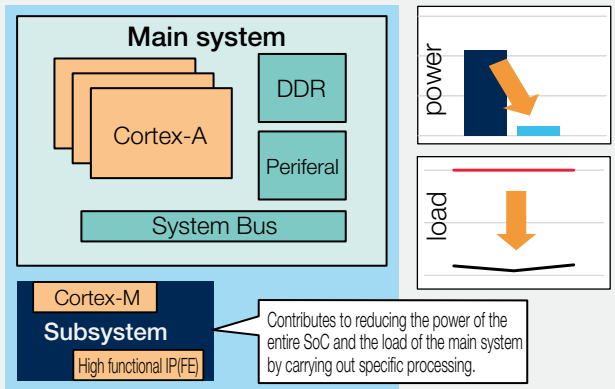
Details of Example Case of Software Platform



Service Category	Service Description	Item Submitted by Customer	Deliverable from Socionext(Example)
Software platform development	OS porting, driver customization,testing	Requirement specifications	Implementation specifications Test specifications and result reports
OS porting	OS porting, testing		
Driver customization	Driver customization, testing		

Provide of Subsystems

Socionext provides original subsystems. These subsystems, which are both high performance and flexible, contribute to the differentiation of customers' products. The key part of the subsystem is the Flexware Engine™, which shares roles with the main system.
To make the introduction of subsystems easier, an SDK (software development kit) is used.



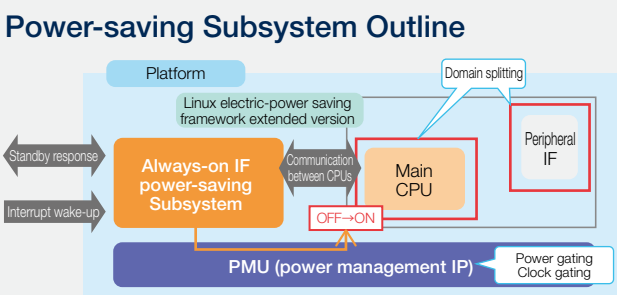
Power-saving Subsystems

●Background and Initiatives

In step with SoCs getting more functional and highly integrated recently, power consumption also tends to increase. At the same time, due to the restrictions on power consumption, as represented by ErP Lot26, and increasing awareness on energy-saving such as the reduction of CO_2 emissions, power-saving is also an important element required for SoCs. Against this background, we have developed a power saving subsystem that satisfies two conflicting elements performance improvement and reduction of power consumption.

●Outline

A power-saving sub-system integrates a high performance IP, ARM micro computer, and peripheral I/O. Operating as an always-on block during system standby, the sub-system saves power in terms of the entire SoC by enabling the main system to be stopped completely. During the standby period, the following processing is performed.

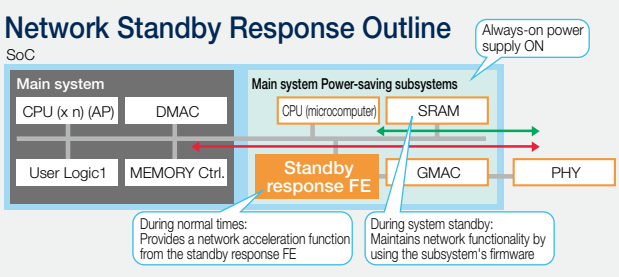


- Network standby response such as Ethernet (to be described later)
- Wake-up control based on notification from USB and other interfaces
- Centralized management of power gating and clock gating

Network standby response

Network standby response is a function in which the subsystem carries out packet processing on behalf of the main system when it is in a standby state. This function also supports the following functions.

- Main system wake-up assistance when a packet requiring processing by the main system is received
- The acceleration function that accelerates packet processing in a normal state



Actual Network Standby Response Performance Values

Functional/Performance	Normal	When proprietary technology is used	Comparison
Stand-by power	2 W to several W	<100mW	<1/20
Communication performance	300Mbps	900 Mbps (20% reduction in CPU load)	Approx. 3 times

Actual measurements with MB86S73 board

Security Subsystem

●Background and Initiatives

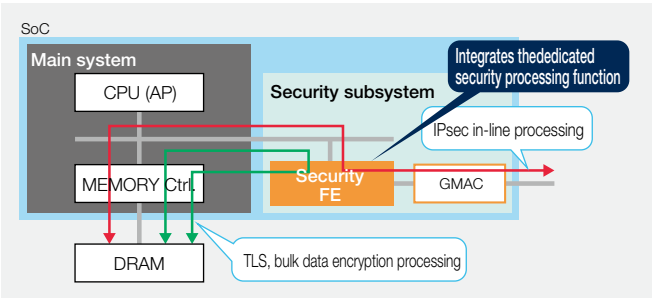
With the recent progress of the IoT (Internet of Things), security functionality is required for various devices. In terms of security functionality, the protection of confidential information stored on network-connected devices and deterrence of unauthorized access or illegal operations are extremely important. Achieving this requires the prevention of software falsification, monitoring by hardware, encryption of the network path, and so on. However, encryption calculation and authentication computing for these security functions impose a very heavy load upon the software. Therefore it is not easy to implement such functionality. To solve this issue, we offer the best subsystem for implementing security functionality.

●Outline

A subsystem based on Flexware Engine™ realizes various encryption authentication functions. In addition to accelerating general-purpose encryption and authentication processing, the subsystem is capable of accelerating complex processes, such as TLS and IPsec. As high load processes are executed by the dedicated hardware, this subsystem achieves 8 to 16 times higher performance compared to software processing.

●Features

- Support for various encryption and authentication algorithms (DES/3DES, AES, ARC4, MD5, SHA1/256/512, etc.)
- Diverse hardware offloading and acceleration functions (TCP/IP checksum, TCP segmentation, IPsec frame, TLS record, etc.)
- Support for the connection of Gigabit Ethernet MAC (optional)
- Acceleration of exponentiation, multiplication, division and remainder calculation required for RSA by a public key encryption calculation acceleration macro (F_PKA) (optional)
- The public key encryption calculation acceleration macro (F_PKA) is also available as a stand-alone macro
- Platform (OS) independent SDK



Supported Algorithms

		IPsec	TLS	Generic
Encryption	DES-ECB / 3DES-ECB			✓
	DES-CBC / 3DES-CBC	✓	✓	✓
	AES-ECB			✓*1
	AES-CBC	✓*1	✓*2	✓*1
	AES-CTR	✓*1		-
	ARC4		✓	✓
	AES-XTS			✓*2
	AES-GCM	✓*1	✓*2	-
Authentication	MD5	✓ (HMAC)	✓ (HMAC)	✓
	SHA1 / SHA256	✓ (HMAC)	✓ (HMAC)	✓
	SHA512			✓
	AES-XCBC-MAC-96	✓*3		-

key length:
*1: 128 / 192 / 256 bit
*2: 128 / 256 bit
*3: 128 bit

Actual Security Subsystem Performance Values

Functional	Normal	Sub System	Comparison
TLS	14.8Mbps	174Mbps	12 times
AES-CBC	78Mbps	1250Mbps	16 times
SHA-1	168Mbps	1380Mbps	8 times

Actual measurements with CA9 board

IP Video Streaming Subsystems

●Background and Initiatives

With the spread of the Internet, the need for video streaming is growing. Typical examples are media servers and network monitoring cameras. In such target areas, this subsystem carries out IP packetization of video data, significantly reducing the processing load of the main system.

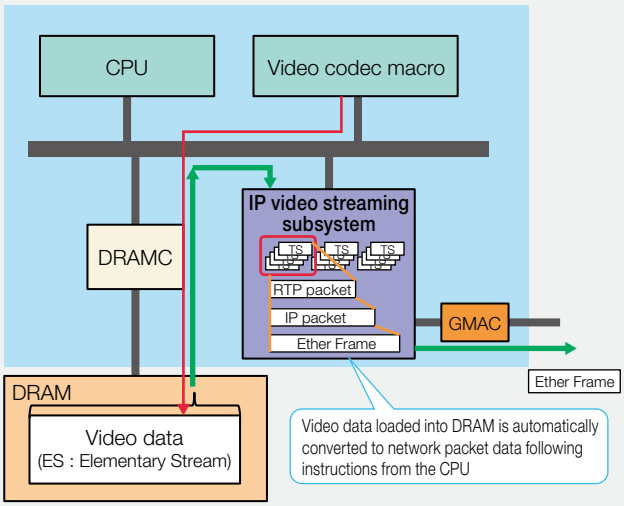
●Outline

Using the Flexware Engine™ as the key part, this subsystem encapsulates video and audio data into an IP packet and encapsulates the IP packet into an Ethernet frame. The following series of processes are performed in the high performance subsystem upon the video data.

- Packetizing video data (ES: elementary stream) into TS packets, if necessary
- Encapsulating ES, TS, or JPEG data into RTP packets
- Encapsulating RTP packets into IP packets
- Encapsulating IP packets into Ethernet frames and performing GMAC control (video transmission)

●Features

- Support for RTP/UDP offloading
  Supported formats
  - ES over RTP : Video (H.264),
    Audio (G.771, AAC)
  - JPEG over RTP
  - TS over RTP
  - Metadata over RTP
- Support for Max.32 streams
- Integration with security (encryption) functionality



Transfer band (Mbps)	10	30	50	150	300	500
Offloading not available CPU load factor (%)	23	62	100			
Offloading available CPU load factor (%)	-	-	15	21	29	39

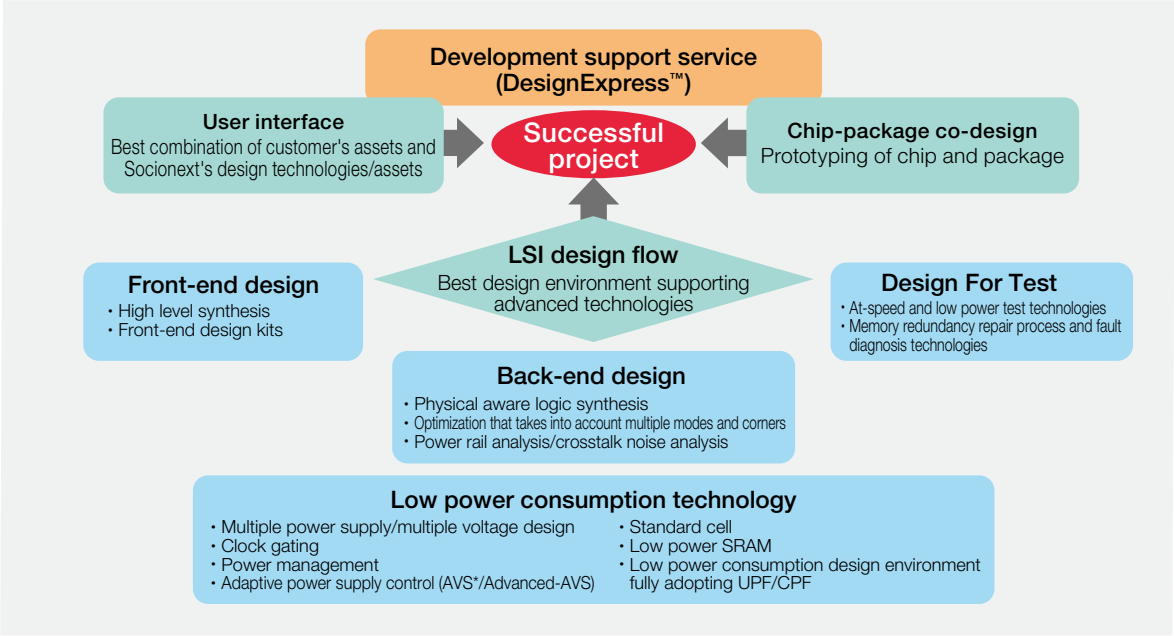
Load reduced by 25 times

Actual measurement of products

Advanced Front-end and Back-end Design Techniques

Design Methodology

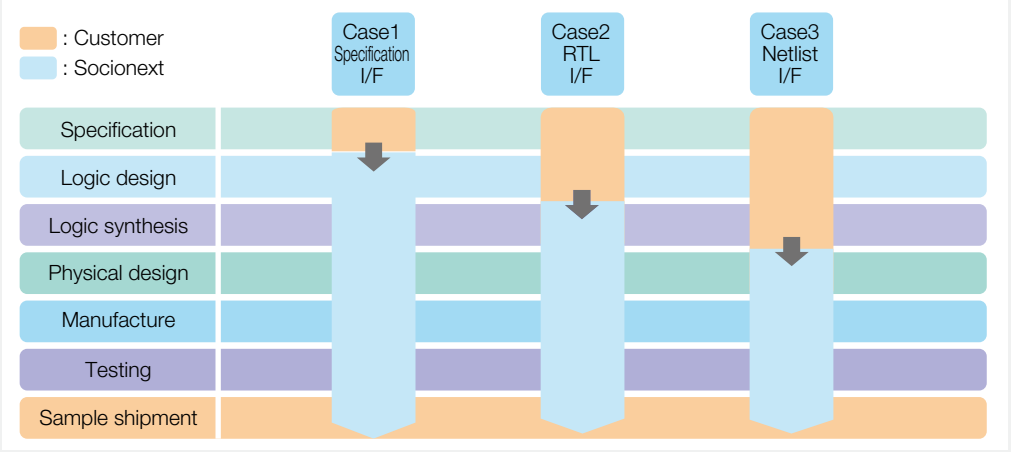
As LSIs become more refined, the number of gates that can be mounted is increasing. In custom SoC development, the demand for chip designs with more than 100-million gates is increasing. It is also becoming important to fulfill the demands of more complicated designs such as reduction of power consumption. In these circumstances, Socionext supports customers in developing LSIs by providing the best design environment needed for each technology.



User Interface

We provide the three types of basic design interfaces shown below as selectable design methodologies.
The optimal combination of customers' design assets and our design technologies and assets improves the efficiency of SoC development projects. We also provide a design flow that incorporates upstream verification and FPGA prototyping, supporting ever higher quality projects and shorter development periods.

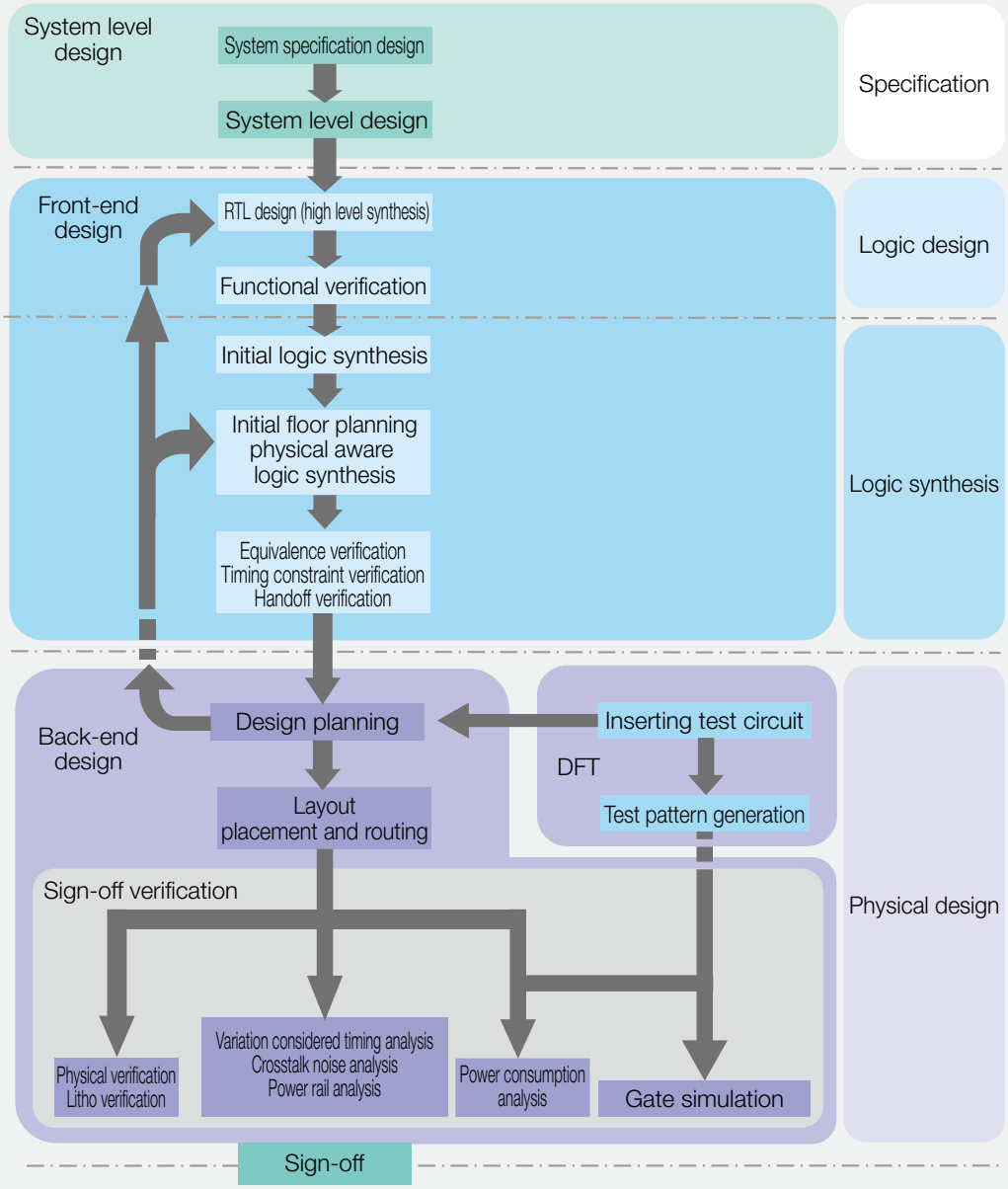
Three Types of Development Interface



Design Flow

We apply an optimized flow based on the following design flow to suit the characteristics of the LSI being developed.

Outline flow of LSI design



Front-end Design

●Front-end Design kit

We offer a development environment using standard EDA tools as a SoC development environment for customers and a tool we created for improving design efficiency as a design kit. The front-end design kit, which is uniquely optimized by Socionext, enables the development of high performance, small chip size, low power LSIs.

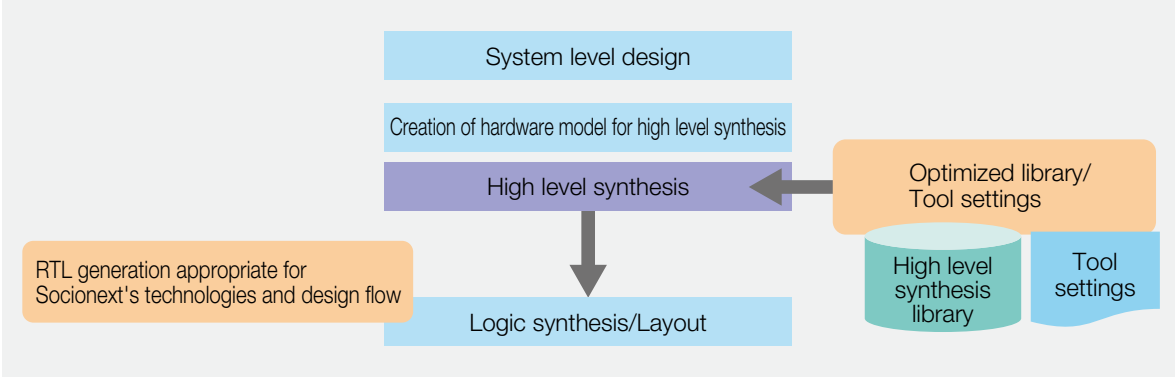
EDA tools supported by Socionext front-end design kit

High level synthesis		Catapult*3, C-to-Silicon Compiler*1, Stratus*1
RTL style check		SpyGlass*2
Functional verification	Verilog-HDL	Incisive Enterprise Simulator*1, Questa*3, VCS-MX,VCS*2
	VHDL	Incisive Enterprise Simulator*1, Questa*3, VCS-MX*2
	CPF/UPF	Incisive Enterprise Simulator-XL*1, Questa*3, VCS-NLP*2
Logic synthesis		Design Compiler*2, Encounter RTL Compiler*1, Genus Synthesis Solution*1
Equivalence verification		Encounter Conformal Equivalence Checker*1, Formality*2
Timing constraint verification		Encounter Conformal Constraint Designer*1, SpyGlass Constraints*2
MV verification		Encounter Conformal Lowpower*1, VC Static Low Power*2
Analysis/debugger		Verdi*2
Netlist check*		SpyGlass*2
Pre-DFT check*		SpyGlass DFT*2

*1: Cadence, Inc.
*2: Synopsys, Inc.
*3: Mentor Graphics Co.
* : We provide a checker we developed in-house to suit the technology.

●High level Synthesis

As chips becomes larger in scale and more complicated, the design environment customers use is also advancing from conventional RTL design to system level design and verification using higher abstraction languages (C++/SystemC). Under these circumstances, it has become common to perform high level synthesis from a high abstraction model to RTL for shorter TAT in RTL design. Socionext provides technology libraries optimized for each high level synthesis tool and documentation describing optimization settings to generate appropriate RTL for our technology and design flow in such high level synthesis.

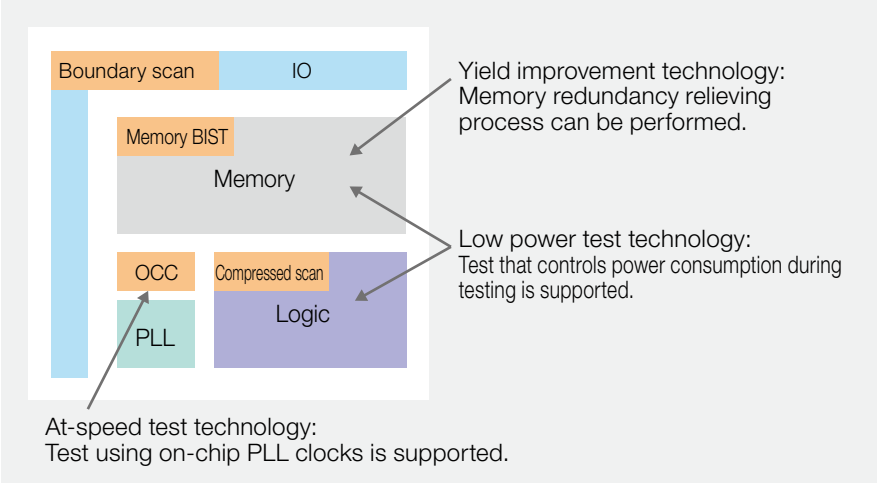


DFT (Design For Test) Technology

SoC testing is becoming more complicated as processes become more refined, circuit scale increases, circuit operation becomes faster, and much less power is consumed. To resolve this issue, in addition to compressed scan, memory BIST, and boundary scan DFT, we perform high quality testing using various types of DFT technology for improved test quality and yield.

[DFT Technologies Adopted by Socionext]

- **At-speed and low power test technologies for improved test quality**
  - Test using on-chip PLL clocks
  - Test that controls power consumption during testing
- **Memory redundancy repair process and fault diagnosis technologies for improved yield**



Back-end Design

We layout customer design with our high-accuracy analysis technology, high performance synthesis, placement, routing, and high speed technology, and low noise design technology.

●Physical aware logic synthesis

Due to the increase in circuit size and routing load caused by the progress of refinement, the gap between the estimate at the time of logic synthesis and layout is widening. At Socionext, we minimize the gap with the layout by taking into account layout information from the logic synthesis step. This allows for early confirmation of timing convergence, thereby shortening the development period.

●UPF and CPF support

We support UPF and CPF and perform physical design and physical verification based on power supply specifications for which functional verification is conducted. This enables high design quality to be achieved even for complex low power consumption technologies.

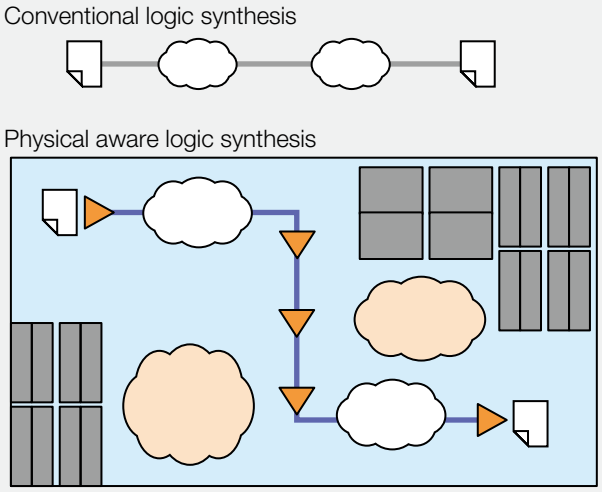
●Multiple mode/corner-aware optimization

As refinement progresses, the processes, voltage, and temperature conditions (corner conditions) that should be taken into account are increasing. In addition, the number of operation modes is increasing to enhance multifunctionality and secure the reliability of LSIs. In our physical design, placement, routing, and optimization that take into account multiple corner conditions and operation modes are performed. This makes it possible to reduce the iteration of timing optimization due to conflicts between different corners and modes, which shortens the development period.

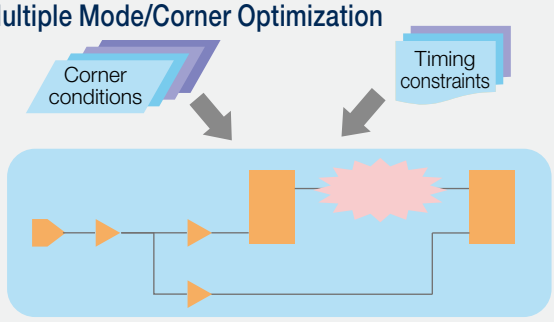
●Power rail analysis/crosstalk noise analysis

As refinement progresses and voltages become lower, the delay variation due to an IR drop (voltage drop) in LSIs and crosstalk noise increases.
Through high accuracy IR drop and crosstalk noise analysis, we have verified that they do not affect system operations.

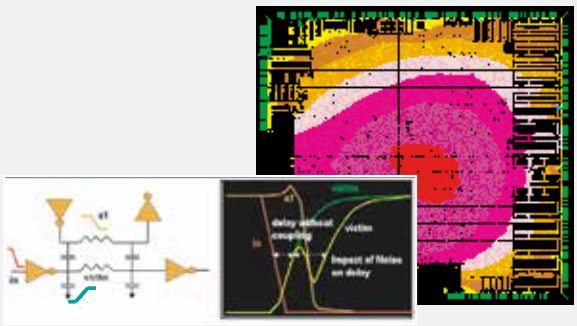
Physical aware logic synthesis



Multiple Mode/Corner Optimization



Power rail analysis/Crosstalk Noise Analysis



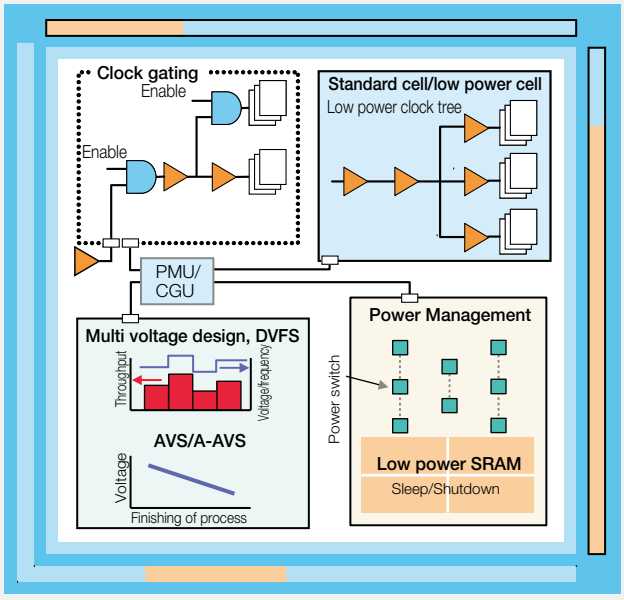
Low Power Design Solutions

The demand for reducing the power consumption of LSIs has been getting stronger in recent years. In our SoC design efforts, we are undertaking various initiatives to meet customers' demands for lower power consumption. In order to achieve low power consumption LSIs, it is effective to combine various kinds of technologies as well as using individual technologies. Socionext's design environment "Reference Design Flow" supports various low power consumption technologies and enables the power consumption of LSIs to be reduced during both operation and standby. By controlling the power supply in particular, we develop methodologies for systematically achieving low power consumption. Also, by fully adopting UPF/CPF, we make low power consumption design, easy for customers while minimizing changes to their design assets. The use of UPF/CPF allows for high reliability designs even with low power consumption technology, which it has been extremely difficult to verify in the past.

●Multi voltage design

With this technology, different voltages are supplied to an LSI to reduce power consumption during the operation of circuit blocks for a high-speed operation circuit block, a high voltage is supplied, and for a low-speed operation circuit block, a low voltage is supplied.
Using UPF/CPF allows physical design and verification of circuit blocks with different voltages to be performed together, minimizing extension of the development period for low power consumption design.

Low Power Design Solutions



Low Power Design Solutions

Design Level	Design Technology		
System level design	Memory access reduction Computation reduction Architecture selection Effective use of cache		
RTL design	RTL optimization	Power Management	Dynamic Voltage and Frequency Scaling
Logic synthesis	Netlist optimization Multi power-supply design Clock gating DVFS, AVS/A-AVS Low power standard cell Low power SRAM		
Layout			

●Clock gating

Clock gating enables the power consumption of LSIs during operation to be reduced by stopping the supply of clock signals to circuit blocks that do not need to operate.

●Power management

We provide power management technology to control power gating, SRAM sleep, and shut-down mode in a comprehensive manner. By thoroughly eliminating useless, this technology contributes to low power consumption. With its unique power switch controlling system, Socionext's power management technology suppresses the rush current noise generated when the power supply is turned on and off to prevent LSIs from malfunctioning.
In addition, using UPF/CPF allows physical design and verification of circuit blocks that have a power shutdown circuit to be performed together, minimizing extension of the development period.

●Adaptive power supply control (DVFS*1, AVS*2/Advanced-AVS)

We can use DVFS, which is for varying the voltage and frequency according to the required throughput.

This technology also adaptively determines the operating voltage according to voltage variation due to manufacturing variability and operates the LSI at the lowest voltage at which its operation is guaranteed, leading to reduced power consumption of the LSI during both operation and standby.

*1: DVFS (Dynamic Voltage Frequency Scaling)
*2: AVS (Adaptive Voltage Scaling)

●Standard cell

In the area of advanced technology, in addition to the standard cell area, routability contributes to the low power consumption of LSIs.We provide our original standard cell that is far superior to that of other companies. In addition, we offer a rich line-up of cells that are effective for achieving low power consumption of the clock system.

●Low power SRAM

An LSI with high-capacity SRAM may have a problem with the power consumption of the SRAM macro. In such cases, power consumption may be reduced by using a multi-mode SRAM. Multi-mode SRAM features a standby mode, sleep mode, and shut-down mode, as well as a normal operation mode. The standby mode allows for the operating power of an SRAM macro to be 0 by stopping the clock operation inside the macro. In sleep mode, leakage power is reduced by deactivating peripheral circuits of the SRAM macro. Power can only be shut down with an SRAM in shutdown mode. The optimization of the SRAM configuration to be used contributes to low power consumption as well. We help customers select the best SRAM from the logic design phase.

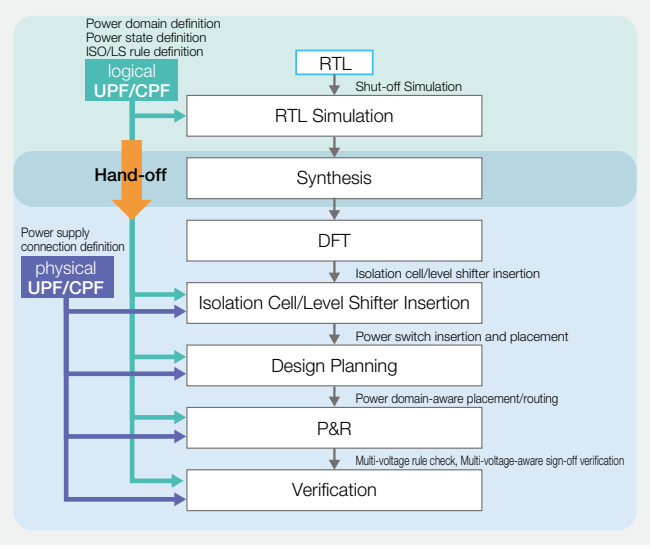
Operating Mode	Function	Effect
Normal	To operate RAM normally	–
Standby	To stop the SRAM operation	The operating power is 0
Sleep	To retain data	Leakage power is reduced to one-third*
Shutdown	To shut down the power with only the SRAM	Leakage power is reduced to one-sixth*

*: Depends on the SRAM structure

●Low power design environment that fully adopts UPF/CPF

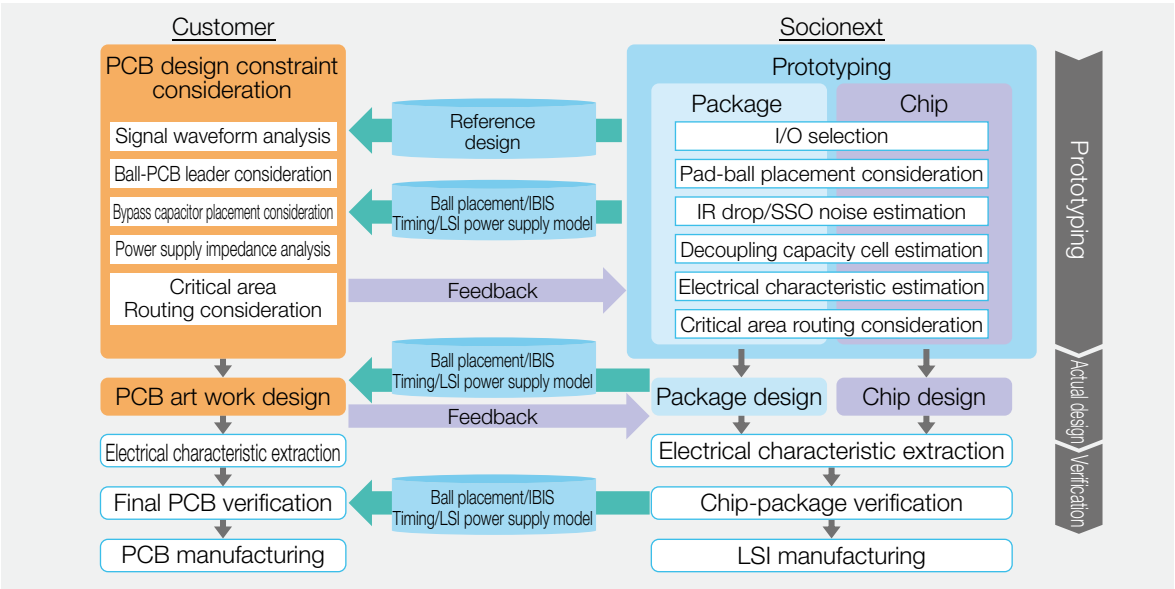
Socionext offers a total solution that supports power gating, multi power supply, and multi-voltage design through consistent power supply specification management with UPF*3 and CPF*4, RTL simulation for complicated power supply design due to an increased number of integrated IPs, multi power supply verification, and physical design. This solution allows power shutdown verification to be performed based on RTL simulation by managing power supply specifications as separate logical and physical specifications and defining only the logical specification. Verified RTL and the logical specification for the power supply are handed off to physical design, the power supply physical specification that defines the power supply connection is prepared, and then physical design is performed based on these power supply specifications(UPF/CPF). Managing the power supply specification with UPF/CPF in this way and using it through a design flow clarifies the power supply specification and allows for high reliability design.

*3: UPF (Unified Power Format) is a standard specification that defines the Low power design guidelines standardized as IEEE Std. 1801. (http://www.ieee.org/)
*4: CPF (Common Power Format) is a standard specification that defines the Low power design guidelines standardized as Si2. (http://www.si2.org/?page=811)



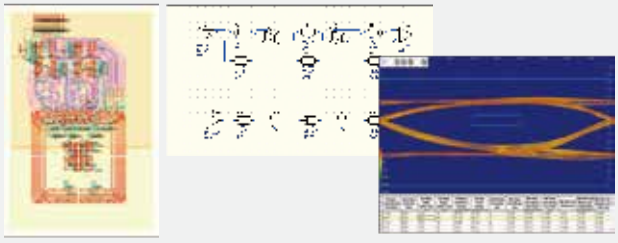
Chips designed with noise in mind, packages, and PCB co-design

Socionext achieves perfect operation on the first attempt through LSI development based on the chip, package, and PCB codesign flow. While offering a good forecast for design through reference design, we develop and improve LSI models (IBIS, timing model, LSI power supply model) necessary for transmission line analysis of DDR4 and other memory interfaces and USB3.0 and other SerDes interfaces to achieve total optimization in each phase of design based on integrated chips, packages, and PCB analysis. This allows for an issue that used to only be discovered in the actual design phase to be addressed in the prototyping phase.

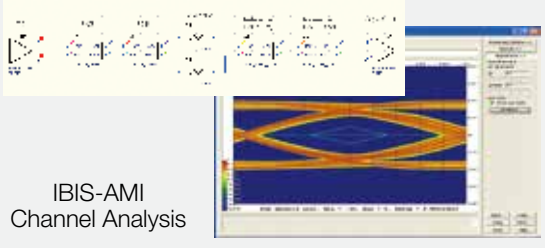


We offer customers IBIS and a timing model early on in the design stage so that they can conduct transmission line analysis taking timing into account.

DDR4 Waveform/Timing Analysis by Customer

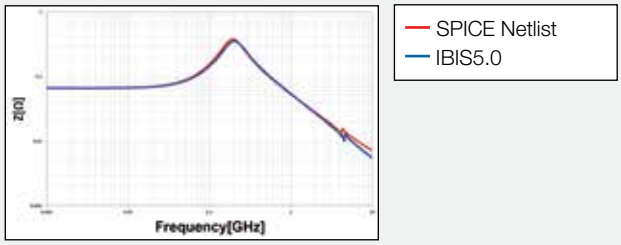


USB3.0 Waveform Analysis by Customer

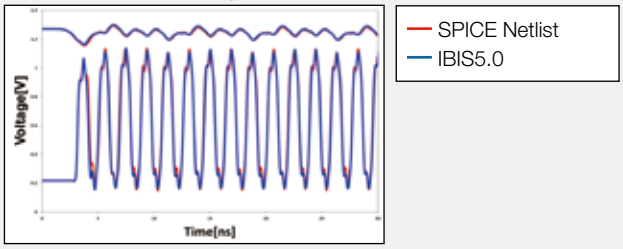


The use of IBIS5.0 and an LSI power supply model (chip and package) for PCB power supply impedance analysis and SSO noise analysis allows customers to perform high accuracy development in a short TAT.

PCB Power Supply Impedance Analysis (SPICE Netlist vs. IBIS5.0)



SSO Noise Analysis (SPICE Netlist vs. IBIS5.0)



Advanced Device Implementation and Manufacturing

Advanced Processes

Technologies and Device Products

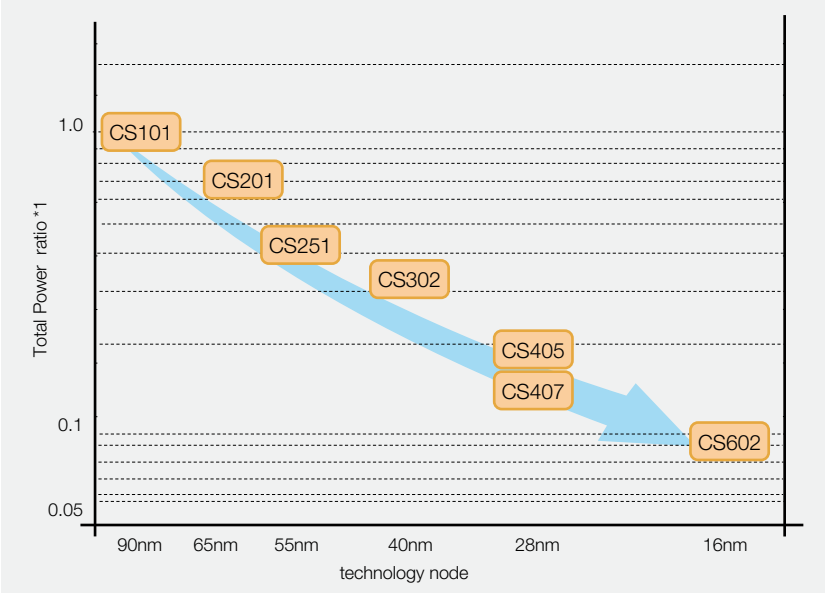
Our device products from 90 nm to 16 nm include standard cell types supporting a wide range of technologies. Socionext is working with multiple foundry partners. Thanks to the synergy effect of their manufacturing capability and the quality control system and design engineering ability of Socionext, we will continue to lead the LSI industry in design and manufacture of cutting-edge custom SoCs using the 28 nm process and beyond.

●Standard cell

Technology	Series	Power Supply Voltage (Typ.)
7 nm FinFET CMOS	T.B.D.	T.B.D
16 nm FinFET CMOS	CS602 series	+0.7V±0.07V / +0.8V±0.08V
28 nm Metal Gate CMOS	CS407 series	+0.8V±0.08V / +0.9V±0.09V
28 nm Metal Gate CMOS	CS405 series	+0.9V±0.09V
40 nm Si Gate CMOS	CS302 series	+1.1V±0.1V
55 nm Si Gate CMOS	CS251 series	+1.2V±0.1V
65 nm Si Gate CMOS	CS201 series	+0.9 V to +1.3 V (supports a wide range)
90 nm Si Gate CMOS	CS101 series	+0.9 V to +1.3 V (supports a wide range)

●Gate scale comparison

●Power consumption comparison



*1 : The vertical axis shows the relative ratio of each technology using the total power (sum of the dynamic component and leakage component) of CS101 as the criterion

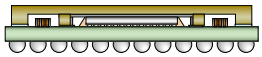
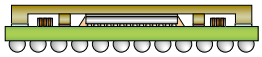
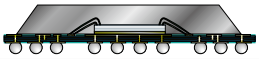
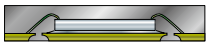
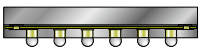
Advanced Packages

Package System

From high performance models for high end use to high cost performance models for consumer use, we provide a wide range of packages.

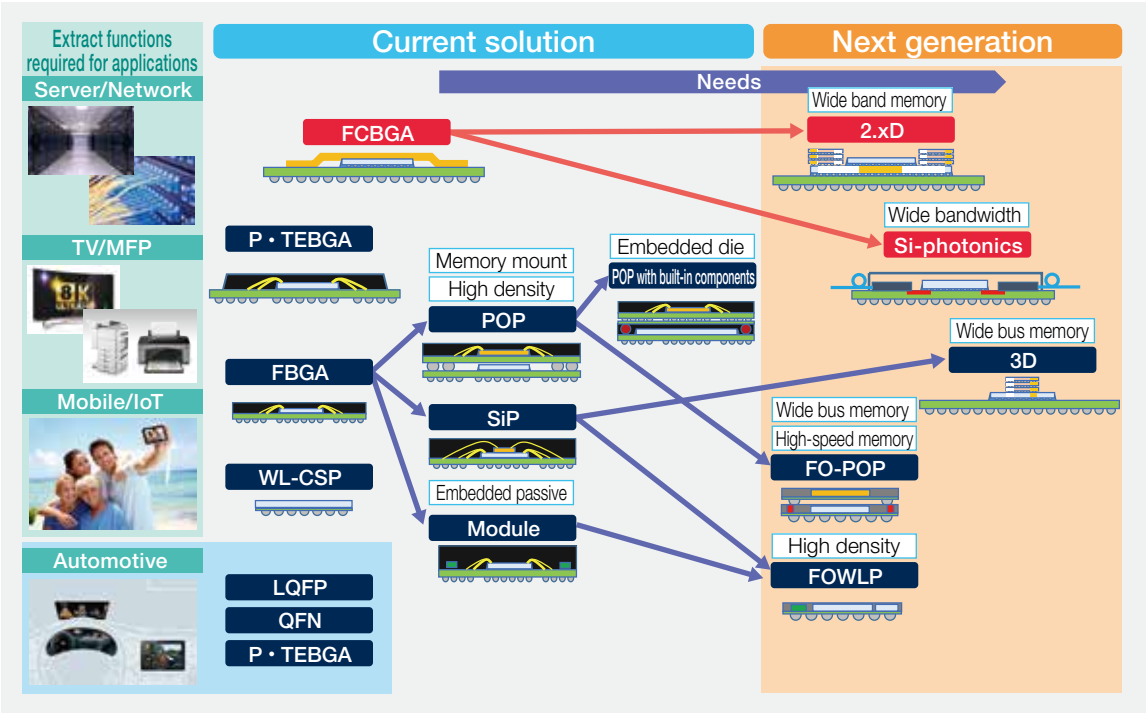
High end

Consumer use

Package Type	Package Structure	Number of Pins	I/O Frequency (GHz)	Thermal Resistor θja (°C /W) (0m/s)	Example Purposes
FC-CBGA		450~2116	~5	7~	Routers, servers, workstations, Broadband communication
FC-PBGA (IVHCore)		450~2116	~2.5	7~	
FC-PBGA (Conventional)		450~1156	~2.5	9~	Routers, computers, graphics, digital TVs, settop boxes, printers
TEBGA		256~1849	~1.6	13~	
PBGA		256~1849	~1.6	15~	
FBGA		up to approx. 1000	~1	17~60	Computers, smartphones, digital video cameras, digital still cameras
QFN		16~88	~1.5	20~40	Smartphones, digital video cameras, digital still cameras
WL-CSP		Approx. 400	~2.5	25~60	
LQFP TEQFP		32~256	~2.5	15~100	Computers, digital TVs, settop boxes, printers

Package Roadmap

Through a strong partnership with outsource assembly and test (OSAT) in Japan and overseas, we provide packages with well balanced technology, cost, quality, and reliability.



Simulation

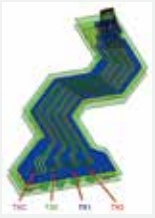
Utilizing advanced simulation technologies, we offer the best package solution.

●Electrical characteristic simulation

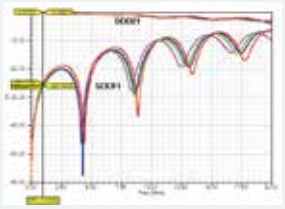
The most appropriate board pattern can be designed based on the results of electrical characteristic simulation.

Case) Electrical Characteristic Simulation of Package Board Wiring

Simulation model



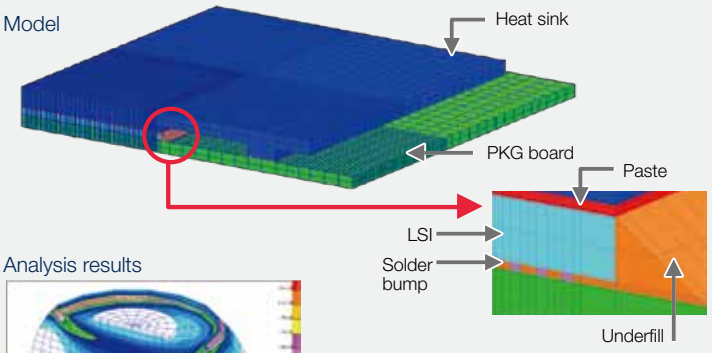
Analysis results



●Mechanism simulation

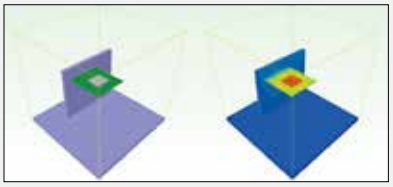
Incorporating mechanism simulation into package design allows customers to propose high reliability packages.

Case) Stress Analysis of Solder Joint Sections

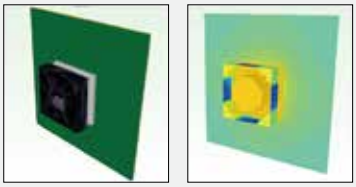


●Thermal design simulation

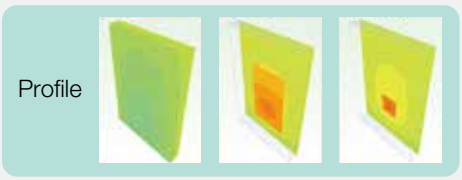
By combining actual measurement of thermal resistors and thermofluid simulation, we perform high accuracy thermal resistance analysis reproducing the operating environment of products. Analysis in an environment defined by the JEDEC standard is also possible.



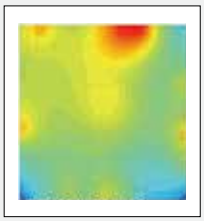
JEDEC Environment



with FIN+FAN



with Heatsink TV Case

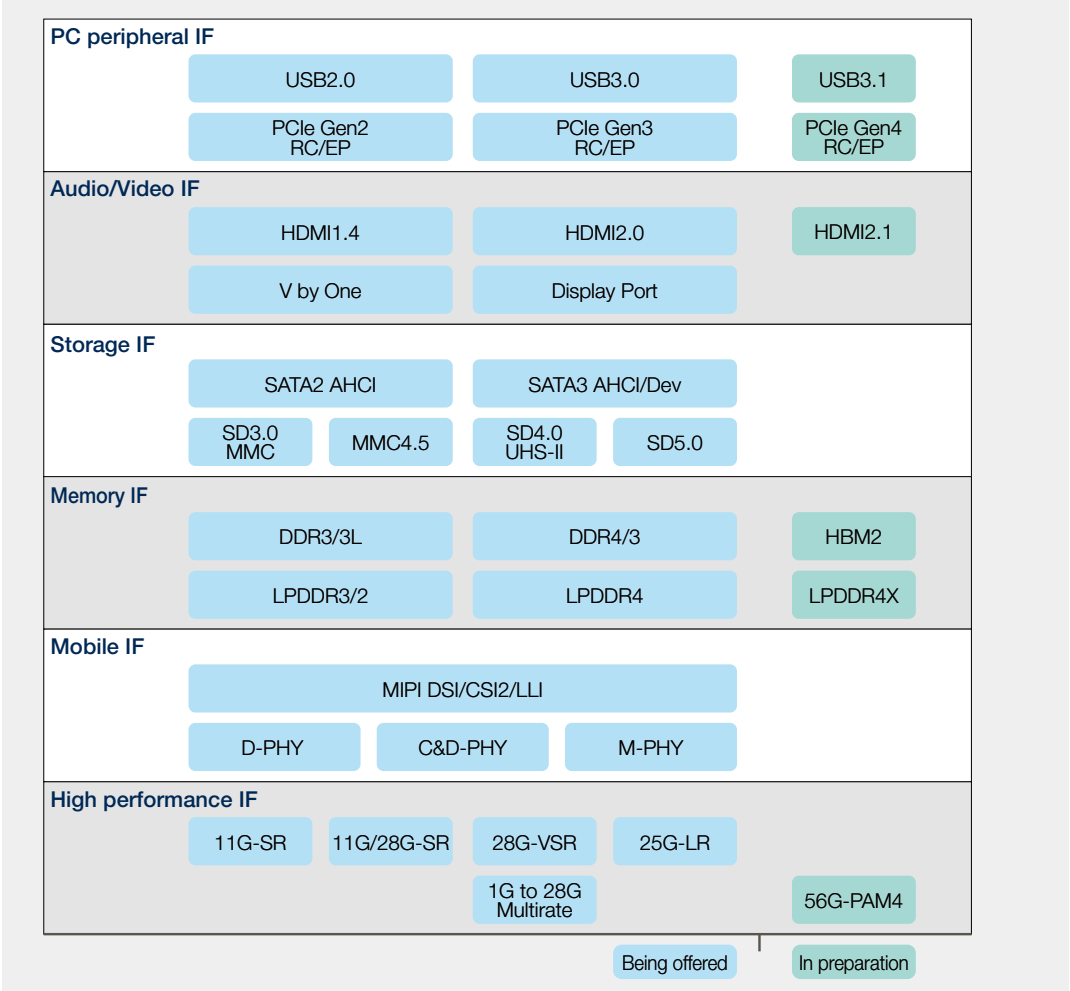


Thermal Distribution on Chip

IP Macros

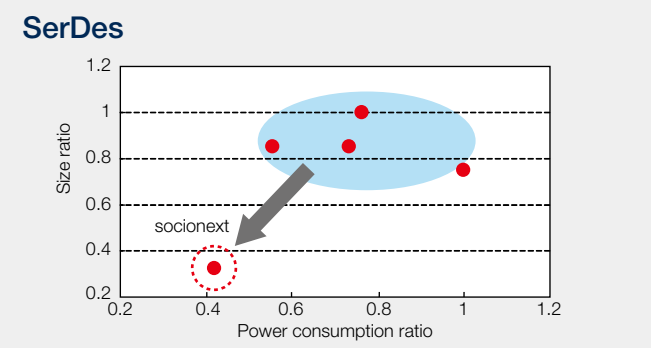
IP Macro Roadmap

Socionext supports customers with the development of advanced SoC by providing high-quality macros verified by its unique IP macro verification system. We develop our own rich IP lineup, which includes CPU, media processing, image processing, and communication interface, and also prepare various types of IP by cooperating with third party vendors, to meet a vast range of customer demands with our cutting-edge technologies. We will continue our development focused on the circuit technology expertise cultivated on the high-end platforms, and provide stable and advanced IPs.



Lower Power Consumption and Smaller IP Macros

As technology advances, system LSIs are increasingly required to have more functions. In response, we have been developing smaller IP macros that consume less power. In addition to reducing power thanks to advances in technology, we provide macros that are available only from Socionext by developing new architectures.



ARM®Solutions

ARM Cores and Design Kits

The comprehensive license agreement with ARM allows customers to select the most suitable ARM core to meet their requirements. We provide the most suitable ARM core and SNAP-DK (design kit), a design environment, for custom SoC for a wide range of applications such as microcontrollers, embedded device, and application equipment.
These ARM cores in the line-up are available on all process technologies that Socionext offers.

Socionext ARM Platform (SNAP)

Use of the SNAP (Socionext ARM based SoC Platform) reduces development time and risks in ARM core-based SoC development. SNAP consist of the following.

●Design Kits: SNAP-DK, ADK, SDK

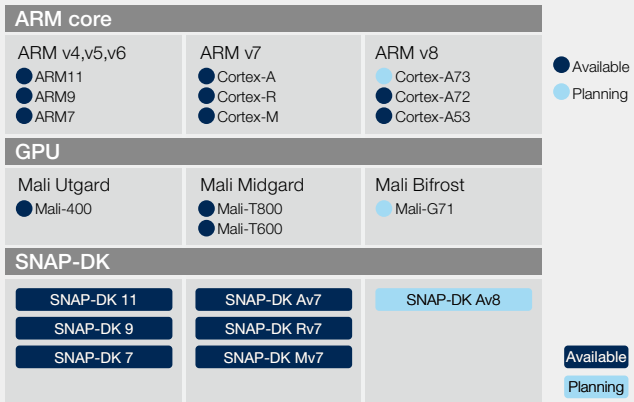
- SNAP-DK : Consists of an ARM core and minimum required peripheral IPs.
- SNAP-ADK : SNAP-DK-based design kit that al-ready implements an interface macro, GPU, etc.
- SNAP-SDK : This design kit provides a fully customized dedicated subsystem for customers using a design tool in accordance with the requirement specifications.

By selecting the most suitable design kit based on the specifications customers require, development time can be reduced significantly.
These design kits, containing a simulation environment, test bench, sample boot code, etc., contribute to the shortening of time to launch the design environment and creation of an appropriate ARM core boot program.

●Prototyping: SNAP-PK

- The SNAP-PK provides Socionext's unique FPGA board with SNAP-DK. By implementing a user logic on the FPGA side, it achieves prototyping of an SoC.
- This product can be used for system operation verification of hardware, performance evaluation, and early development of software.

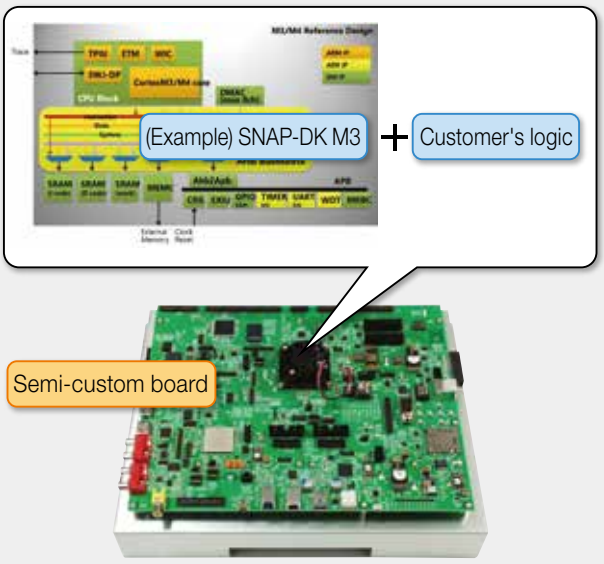
Line-up of ARM cores, GPUs, and SNAP-DKs



SNAP Design Kits

Type	Content	Advantage
SNAP-DK (Basic Design Kit)	CPU + small-scale peripheral IPs	Bootable CPU subsystems can be used
SNAP-ADK (Advanced Design Kit)	SNAP-DK + high performance IPs (system with guaran-teed performance)	High performance CPU subsystems including an OS can be used
SNAP-SDK (System Design Kit)	Consultation-based full custom design kit (system with guaran-teed performance)	Dedicated subsystems based on requirement specifications and existing systems can be used

SNAP-PK



●Driver/OS: SNAP-Linux

SNAP-Linux provides the Linux kernel for which operation has been checked on the SNAP-PK and various IP drivers.

This product contributes to reducing software development time for customers.

SNAP (Socionext ARM Platform)

Interface Macros

DDR Interface

Socionext provides various DDR interface macros from low-to-middle speed forwarding bandwidth to high-speed forwarding bandwidth or low power, with various process technologies.

Moreover, we support custom SoC development by LSI-Package-Board co-design.

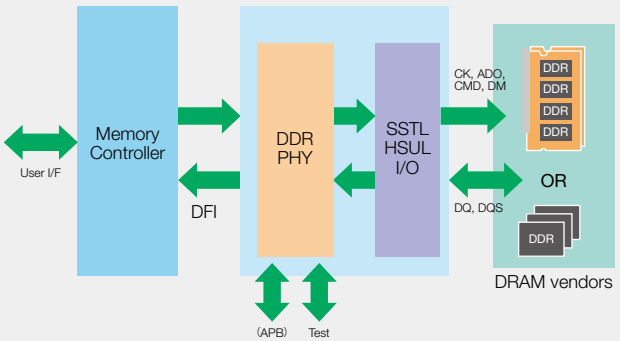
●DDR interface macros

- High-speed/high-bandwidth　DDR3/DDR4
- Low power　LPDDR4/LPDDR3/ LPDDR2/DDR3L
- DFI compliant (all macro)
- Compatible with many different DRAM configurations and PKG options, such as Fly-by and PoP thanks to the PHY function (training function).

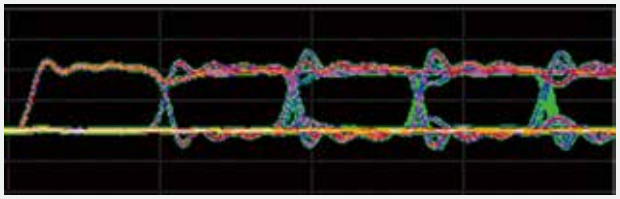
●DDR interface design support (LSI-Package-Board codesign)

- Timing verification : Verifies the timing of all DDR-IF systems including delays between LSI I/O and DRAM
- Power Integrity : Optimizes the parasitic inductance, resonant frequency, and power supply (PKG, PCB) impedance as part of the power supply impedance design
- Signal Integrity : Optimizes Driver strength, terminator resistance, and interconnect topology

DDR Interface Configuration Diagram



LPDDR4-2400 DQ Waveforms



Memory Controllers

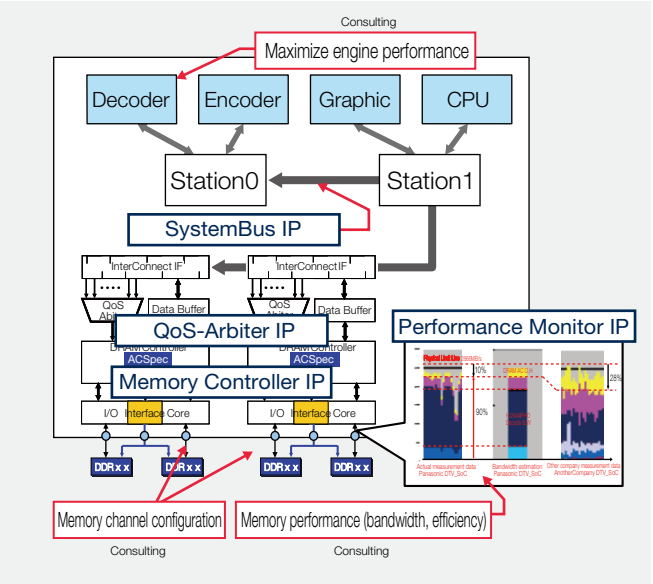
Socionext provides various memory solutions for system optimization. We also offer consulting services on memory systems including memory channels and the system bus to maximize SoC performance.

●Memory controller IP
- Controller for maximizing high DRAM utilization

●QoS-Arbiter IP
- High performance QoS-Arbiter featuring multiple functions

●BusIP
- Original low power consumption bus with high layout flexibility

●MonitorIP
- Visualizes memory system performance in real-time
- Monitors performance (bandwidth, latency) and provides an environment for tuning parameters



SLVS-EC Interface

This is a high-speed interface for constructing a camera system with a high-speed, high-resolution CMOS image sensor.

With a high bandwidth of up to 18.4 Gbps, this interface provides a solution for fully expressing images.

●SLVS-EC macro
- Supports up to 8 times the number of lanes
- Integrates Reed-Solomon ECC
- Multiple stream transfer can be selected

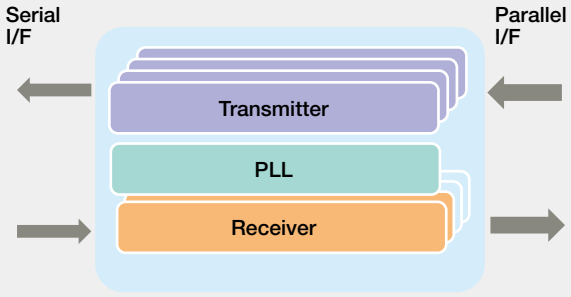
SLVS-EC Evaluation Board

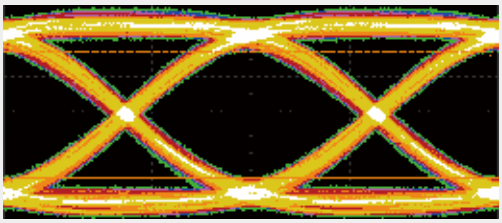
10G-28Gbps SerDes Interface

With transmission performance of 10Gbps–28Gbps per channel and a configuration comprised of multiple channels, we provide a high-performance SerDes macro for constructing 100G/200G/400G optical networks or 100G Ether systems.
The built-in low-jitter, high-performance PLL enables robust transmission up to 28 Gbps per channel.
It also supports various standards including OIF-CEI-11G-SR, OIF-CEI- 28G-SR, OIF-CEI-28G-VSR, IEEE802.3ba CAUI, IEEE802.3bm CAUI4, XFI and so forth.

×1, ×4 lane configuration.

- Comprised of Transmitter/Receiver/PLL and capable of bidirectional communication with 1 macro.
- Up to 112.8 Gbps per macro (for unidirectional, ×4 configuration).
- Support for power-down control on each lane.
- Support for power-down control for the entire macro.
- Implementing Clock-Data recovery for each Receiver lane.
- Transmitter Equalization supported.
- Receiver Equalization supported.





28 Gbps Output Waveforms with Test Chip

- Built-in termination resistor in Transmitter/Receiver.
- Organic flip chip package.
  (0.8 mm/1.0 mm Ball Pitch, HDBU Package)

Analog Macros

We offer various analog macros (data converter, power management, temperature sensor, analog front-end) for our customers' development to address various applications including communication, image processing, sensors and control.

- All macros are silicon verified.
- Implemented on many custom SoCs with a track record in mass production.

Data Converters

We offer various data converter macros addressing low power consumption and a small area which are demanded in SoCs.

●Pipeline & high speed SAR ADC

- 10-bit/12-bit resolution, maximum 200MSPS conversion rates
- The world's smallest class power consumption

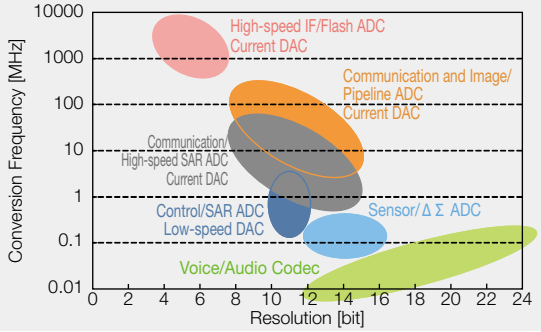
●ΔΣ ADC

- Applicable to 16bit to 24bit resolutions
- Power consumption of up to 1 mW with high precision SINAD 85 dB

●ΔΣ DAC

- Applicable to 16bit to 24bit resolutions
- SINAD 90 dB. Power consumption is 1 mW or less

Data Converters



Power Management

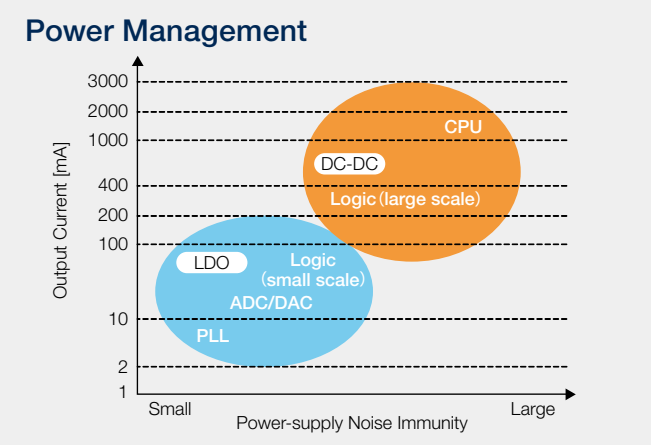
We offer various power management macros that enable single power supply development which is demanded in SoCs.

●DC-DC converter for large current supply applications

- Reduced cost achieved by consolidating power-supply IC functions in SoCs
- 85% power conversion efficiency
- Safety protection functions such as short-circuit detection implemented

●LDO for low noise power supply applications

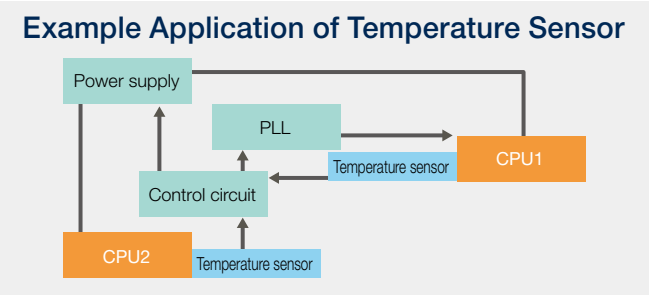
- Line-up of small area version such as integrated I/O type
- Safety protection functions such as short-circuit detection implemented
- Power supply to analog IPs such as ADC and PLL supported



Temperature Sensor

We offer temperature sensor macros for voltage and frequency control according to chip temperature.

- Chip temperature monitoring at a high resolution (0.125℃ step) enabled by the built-in high accuracy ADC
- Multiple sensors installed on one chip due to low power consumption and small area

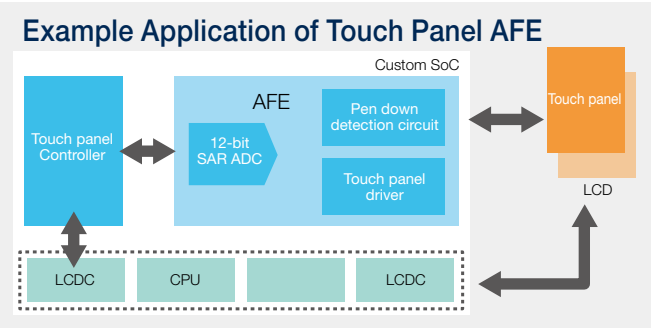


Analog Front-End (AFE)

We offer low power consumption AFEs for processing various sensor signals.

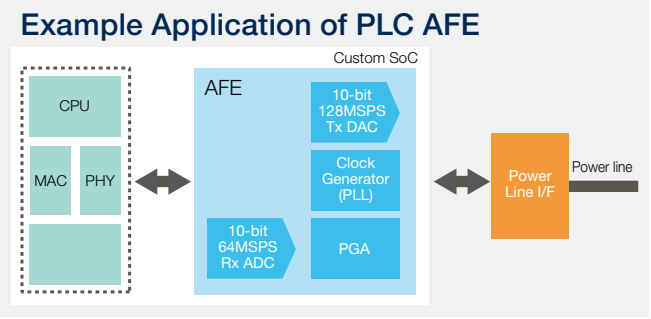
●Touch panel AFE

- Suitable for 4-wire resistive film touchscreen panels
- Built-in driver circuit for operating resistive films
- 12-Bit SAR ADC installed
- Touch position detection, pen pressure detection and pen interrupt functions supported



●Scanner AFE

- Both CCD and CIS supported
- Gain and offset adjustment function implemented
- 12-bit high-speed ADC installed
- Low power consumption (72mW)



●Power line communication (PLC) AFE

- High-speed PLC standards (HD-PLC, IEEE1901, etc.) compliant
- High accuracy and high-speed ADC/DAC circuits installed
  Transmitter : 10-bit 250MSPS 3.3V DAC
  Receiver : 10-bit 125MSPS 1.2V ADC
- Low power consumption (365mW)

Line-up of IP Macros

Socionext's IP macros with their proven track records support customers in advanced SoC development.

●Functional/Interface Macros

Category	Function	Process Technology					
		90nm	65nm	55nm	40nm	28nm	16nm
ARM Cores	Cortex-A	✓	✓	✓	✓	✓	✓
	Cortex-R	✓	✓	✓	✓	✓	✓
	Cortex-M	✓	✓	✓	✓	✓	✓
	ARM11, ARM9, ARM7	✓	✓	✓	✓	✓	✓
	Mali	✓	✓	✓	✓	✓	✓
Image Core	JPEG	✓	✓	✓	✓	✓	✓
	H.264	✓	✓	✓	✓	✓	✓
	H.265	✓	✓	✓	✓	✓	✓
Security Core	MD5/SHA	✓	✓	✓	✓	✓	✓
	PKA	✓	✓	✓	✓	✓	✓
	DES	✓	✓	✓	✓	✓	✓
	AES	✓	✓	✓	✓	✓	✓
	IPSEC*	✓	✓	✓	✓	✓	✓
	TLS*	✓	✓	✓	✓	✓	✓
Interface Controller Core	IrDA	✓	✓	✓	✓	✓	✓
	UART	✓	✓	✓	✓	✓	✓
SD	UHS-I	✓	✓	✓	✓	✓	✓
	UHS-II					✓	✓

* : For details, refer to security subsystems on page 15.

●High Speed Interface Macros

Category	Function	Process Technology					
		90nm	65nm	55nm	40nm	28nm	16nm
USB	USB3.1 Gen2 Host/Device					✓	✓
	USB3.1 Gen1 (USB3.0) Host/Device		✓	✓	✓	✓	✓
	USB2.0 Host/Hub/Device	✓	✓	✓	✓	✓	✓
Ethernet	Gigabit Ethernet MAC	✓	✓	✓	✓	✓	✓
Video	HDMI2.0	✓	✓	✓	✓	✓	✓
	V-By-One HS				✓	✓	
	FPD-Link	✓	✓	✓	✓	✓	
LVDS	LVDS	✓	✓	✓	✓	✓	✓
	SubLVDS	✓	✓	✓	✓	✓	✓
MIPI	DSI	✓	✓	✓	✓	✓	✓
	CSI-2	✓	✓	✓	✓	✓	✓
	LLI					✓	
	D-PHY	✓	✓	✓	✓	✓	✓
	C/D-PHY					✓	✓
	M-PHY					✓	✓
PCI Express	PCIe Gen3 RT/EP					✓	✓
	PCIe Gen2 RT/EP		✓	✓	✓	✓	
	PCIe Gen1 RT/EP	✓					

(continued on the following page)

●High Speed Interface Macros

Category	Function	Process Technology					
		90nm	65nm	55nm	40nm	28nm	16nm
Serial ATA	SATA3 AHCI				✓	✓	
	SATA2 AHCI	✓	✓	✓	✓		
	SATA3 Device				✓		
DRAM Interface (PHY)	DDR3	✓	✓	✓	✓	✓	✓
	DDR3L	✓	✓	✓	✓	✓	✓
	DDR4				✓	✓	✓
	LPDDR3				✓	✓	✓
	LPDDR4					✓	✓
	HBM2						✓

●Analog Macros

Category	Function	Process Technology					
		90nm	65nm	55nm	40nm	28nm	16nm
ADC	8bit, up to 140MSPS	✓	✓	✓	✓	✓	
	10bit, up to 200MSPS	✓	✓	✓	✓	✓	
	12bit, up to 200MSPS	✓	✓	✓	✓	✓	✓
	16bit	✓				✓	✓
DAC	10bit, up to 220MSPS	✓	✓	✓	✓	✓	
	12bit, up to 110MSPS	✓	✓	✓	✓		
	16bit	✓	✓	✓			
AFE	Audio				✓	✓	
	Video				✓	✓	
	Scanner				✓	✓	
	Touch Panel	✓	✓	✓			
Temperature sensor	+/-5deg.C accuracy (without trimming)		✓	✓	✓	✓	✓
Regulator	Vin=3.3V, Vout=1.0-1.2V, Iout≦200mA LDO	✓	✓	✓		✓	
	Vin=3.3V, Vout=1.0-1.2V, Iout≦400mA DCDC	✓	✓	✓			
Standard PLL	Fout: ~1200MHz, Fin:10~200MHz	✓	✓	✓	✓	✓	✓
	Fout: ~1600MHz, Fin:16~200MHz	✓	✓	✓	✓	✓	✓
	Fout: ~5000MHz, Fin:20~100MHz					✓	✓
Low Jitter PLL	Fout: ~600MHz, Fin:11~100MHz	✓	✓	✓	✓		
	Fout: ~6000MHz, Fin:20~100MHz					✓	✓
Fractional -N PLL	Fout: ~1600MHz, Fin:10~50MHz	✓	✓	✓	✓		
	Fout: ~2800MHz, Fin:10~50MHz					✓	✓
SSCG	Fout: ~1600MHz, Fin:10~50MHz	✓	✓	✓	✓		
	Fout: ~2800MHz, Fin:10~50MHz					✓	✓

Socionext Inc.

Nomura Shin-Yokohama Bldg., 2-10-23 Shin-Yokohama,
Kohoku-ku, Yokohama, Kanagawa, 222-0033, Japan
Tel. +81-45-568-1015

http://socionext.com/en/

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