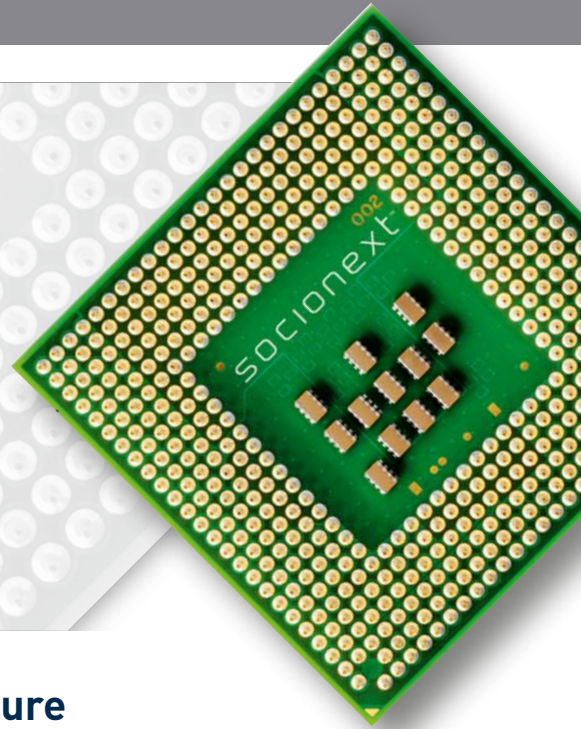


SEERIS® Graphics Engine IP

Scalable Building Block Concept



- 2D/2.5D Rendering
- Display Engine
- Video Capture Engine
- Safety Features



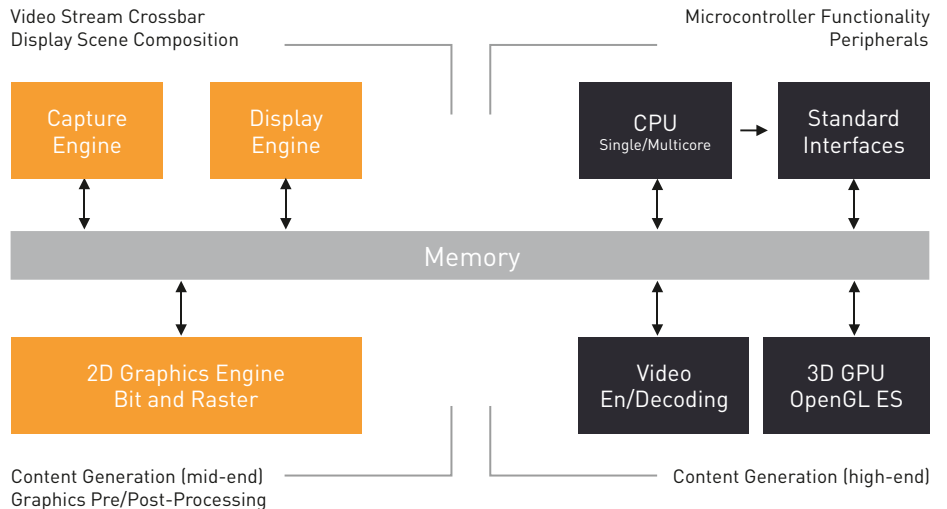
Unified Engines for Graphics, Display and Capture

In order to drive visual and animated graphics the SEERIS® engines provide multiple blocks that can be configured to customer needs. The visual content created by the operating system can be processed into a final image displayed on multiple screens.

The efficient system architecture allows the combination of graphics such as videos, pictures, icons or 3D graphics rendered by the GPU. General features consist of 10-bit per color processing, up to 4k resolution and shadowed register configuration. Industry-leading cost-efficient IP for graphics is able to drive the visual experience across a wide range of SoCs and is capable of working with different screen types, sizes and resolutions.

Additional features like a signature unit and/or CRC counters support safety critical use cases. These high-performance engines are de-

signed for consumer, embedded and automotive applications. Their architecture offers complete scalable modules or subsystem solution IPs.



Automotive

- Instrument Clusters
- Multimedia and Infotainment
- Driver Assistance Systems



Consumer

- Smart Devices
- Digital Cameras
- Internet of Things

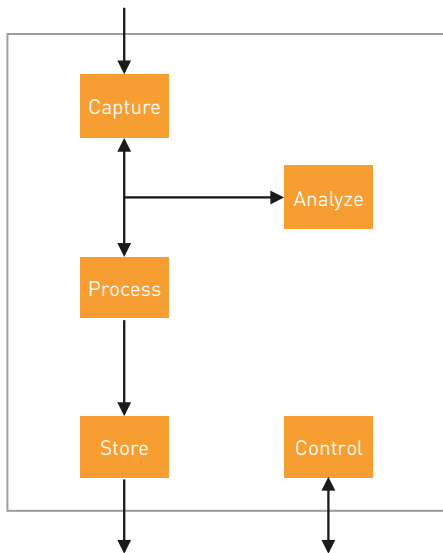


Embedded

- Connected Home
- Healthcare
- Home Electronics

SEERIS[®] Graphics Engine IP

Video Capture Engine



Input Capturing

- 32-bit parallel RGBA or YUV 4:4:4 / 4:2:2 (HSync, VSync, Data enable, Field polarity)
- ITU 656 (Interlaced YUV 4:2:2)

Video Analyze

- Timing Detection
- Histogram Measurement

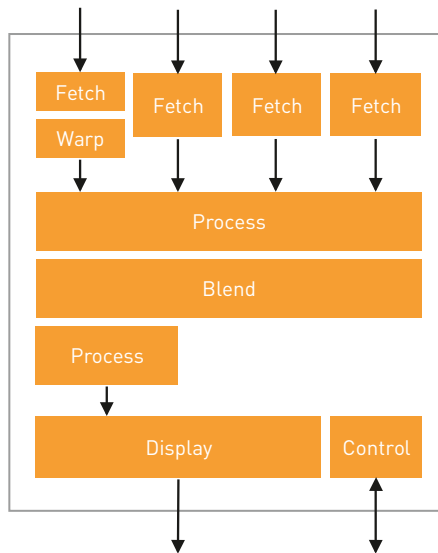
Stream Processing

- Gamma Correction
- Linear Color Operation
- Down-Scaling

Buffer Storing

- RGBA, YUV or Compressed Format
- De-Interlacing by Line Insertion ("Weave")
- Support for Fractional Ring Buffer Size (Optimized Memory Layout)

Multi Layer Display Engine



Buffer Fetching

- RGBA, YUV or Compressed Format
- Packed and Planar Mode
- Flip, Mirrored or Rotated
- Warping
- Support for Fractional Ring Buffer Size (Optimized Memory Layout)

Stream Blending

- 4 Streams
- Alpha Blending

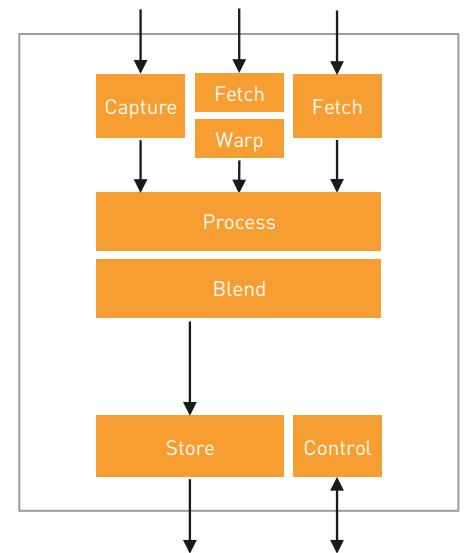
Stream Processing

- Linear Color Operation
- Up-Scaling

Display Processing

- Safety Layer Overlay
- Panic Mode Fallback
- Gamma Correction
- Dither Operation
- Signature Calculation

2D Pixel Processing Engine



Buffer Fetching

- RGBA, YUV or Compressed Format
- Packed and Planar Mode
- Alpha Layer
- Flip, Mirrored or Rotated
- Arbitrary Warping
- Perspective Warping (2.5D)

Stream Processing

- OpenGL/VL/WF Compliant Blending
- Rop, any Logic Operation
- Scaling
- FIR Filter Operation, (5x5)
- Non-Linear Color Correction
- Linear Color Operation

Buffer Storing

- RGBA, YUV or Compressed Format

About Socionext Inc.

Socionext is a new, innovative enterprise that designs, develops and delivers System-on-Chip products to customers worldwide. The company is focused on imaging, networking and other dynamic technologies that drive today's leading-edge applications. Socionext combines world-class expertise, experience, and an extensive IP portfolio to provide exceptional solutions and ensure a better quality of experience for customers. Founded in 2015, Socionext Inc. is headquartered in Yokohama, and has offices in Japan, Asia, United States and Europe to lead its product development and sales activities.

For more information, visit socionext.com.

For more information on our graphics products visit socionext-graphics.com

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