Custom SoC (ASIC)
Custom SoC Solutions create New Value on your Next-Generation Products

With increasing functionality and higher performance of SoC, it is becoming more and more complicated to develop SoCs in a short time. Over the past 40 years, Socionext’s Custom SoC Solution BU has earned reputation of being able to develop custom SoCs that meet our customers needs. Using our techniques of system architecture design, development support services, software platform, and customizing our ASSPs as core, we develop "One Step Ahead" system with you. We believe our role is to propose and provide custom SoC solutions that create new value in next generation products.
With increasing functionality and higher performance of SoC, it is becoming more and more complicated to develop SoCs in a short time. Over the past 40 years, Socionext’s Custom SoC Solution BU has earned reputation of being able to develop custom SoCs that meet our customers needs. Using our techniques of system architecture design, development support services, software platform, and customizing our ASSPs as core, we develop “One Step Ahead” system with you. We believe our role is to propose and provide custom SoC solutions that create new value in next generation products.
Custom SoC Solution

Custom SoC Solutions Overview

As for System on Chip (SoC) with CPU core, nowadays, various and highly functional SoCs development are demanded for a wide variation of CPU cores, high-performance buses, high-speed interfaces, and multi-functional IPs.

At the same time, for optimized customer’s applications, it is becoming much complicated to select the best combination of components from the large number of combinations and it is becoming more harder to develop SoC in a short time. To deal with this situation, Socionext offers a "Custom SoC Solution" which integrates our development methodologies for ease of development, various platforms and development support services. Our "Custom SoC Solution" helps you to achieve high-performance and high-quality SoCs for your products in a short term.

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<th>System architecture design support</th>
<th>Development methodology</th>
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<td>Development support service</td>
<td>Software platform</td>
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<tr>
<td>Advanced Front-end Back-end technology</td>
<td>Base platform</td>
</tr>
<tr>
<td>High reliability testing technology</td>
<td>Application IP/Subsystem</td>
</tr>
<tr>
<td>Advanced device implementation and manufacture (Partner Collaboration)</td>
<td>IP macro</td>
</tr>
<tr>
<td></td>
<td>Standard cell</td>
</tr>
</tbody>
</table>

Development Methodology for Custom SoC Solutions

We provide four development methodology options for custom SoC solutions depending on the customer’s application development period and budget.

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<thead>
<tr>
<th>Development Methodology for Custom SoC Solutions</th>
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<tbody>
<tr>
<td>ASSP based Development</td>
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<td>Customizing our ASSP and combining with a variety of IPs</td>
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<tr>
<td>Platform based Development</td>
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<td>Developing based on our proven platform</td>
</tr>
</tbody>
</table>
ASSP-based Development

By customizing Socionext’s ASSP (Application Specific Standard Procedure) products and combining with a variety of IPs, customer can reduce the development period for custom SoC and accelerate the product shipment.

General-purpose Processor-based Development

We provide general-purpose processors for developing a high-performance, low power consumption system with high-performance CPUs and GPUs as well as high-speed interfaces at a low cost in a short time. We consider these general-purpose processors as a platform SoC.

By combining customer’s functional logic with our platform SoC, we reduce development risk of processor peripheral and high-speed I/Os and developing cost is also reduced significantly. It is also possible to integrate these system components into a single package with an optional SiP (system in a package) technology.
**Platform-based Development**

For your low risk development, we use platform SoC with a proven track record. After trimming unnecessary IPs and I/O’s from our base platform SoC, we combine this trimmed parts and your customer’s logic into a single chip. You reduce re-make risk and development period significantly by 1. using our evaluation kit, 2. preliminary software development, 3. hardware development based on proved platform SoC, and 4. whole chip verification using semi-custom board.

**Full Custom Development**

To achieve the best performance of your SoC, we have full custom development option that allows you to customize as you like. For your full custom SoC development, we fully support for 1. proposing system architecture, 2. providing subsystem and a various of IPs, 3. optimized CPU peripheral design, and 4. system verification by hardware emulator and FPGA prototype. We also provide a device driver development service under contract as part of our software development support.
Example of ASSP-based Development

This section introduces one example of ASSP-based development.

1. Extracting necessary application IP from ASSP
   We extract application IPs which are required for customer’s development from our proven ASSP.

2. Combining base platform and extracted application IP
   After cutting down unnecessary IPs and Interfaces from base platform, then we combine this optimize platform and extracted application IP.

3. Adding your special functions to differentiate from others
   By adding your special functions to differentiate from others, your special SoC design is now created.
Evaluating and verifying functions, performance, and power
The functions, performance, and power can be evaluated and verified using a dedicated hardware emulator at approximately 1000 times as fast as an HDL simulator.
For your software development, we provide a prototype environment such as an FPGA board and CPU board. This allows customers to develop software before manufacturing SoC.

PCB (printed circuit board) co-design
Implementing high-speed components (DDR, PCIe, USB, etc.) and SoC on a PCB tends to cause a electrical issue such as electromagnetic noise, crosstalk, and clock jitter. We analyze such issue creating PCB prototype and offer proposed measures.
This reduces risk associated with developing a PCB and thereby reduces cost for PCB design and manufacturing.

Benefits of ASSP-based Development
From our experience of ASSP-based design for our product, the development period was achieved six months shorter than the development period by conventional design. This rapid time-to-market was achieved by shortening hardware design period and by developing software in advance.

- Delivery time of sample SoC: Six months ahead of schedule
- Advance development of software: Eight months ahead of schedule
- Product shipping: Six months ahead of schedule
Development Support Service (DesignExpress™)

This design service provides consistent development support for everything from system specification to evaluation as well as for PCB design in custom SoC development for our customers. With this service, our customers can focus on differentiating their products while shortening the development period, reducing development risks, improving product quality, and reducing power consumption.

List of Development Support Services

- Advance development of software and performance evaluation service in a virtual environment (Cedar™-ESL)
- High level synthesis support service (Cedar™-HLS)
- Logic design service
- High-speed logic verification and power consumption computing service using emulators (Cedar™-EMU)
- Prototype board development service (Cedar™-PROT)
- PCB co-design support service (PLACATE™)
- Software development service
- Provide of subsystems
Advance development of software and performance evaluation service in a virtual environment (Cedar™-ESL)

Cedar™-ESL is used to develop software in advance using ESL technology (virtual platform) and also for software driven performance evaluation and architecture evaluation. Software driven performance evaluation and architecture performance evaluation allow for architecture design to be performed at an early stage.

**Example applications of Cedar™-ESL**

- Division of functions between hardware and software enabled by advance development of software
- Architecture design and use case extraction based on software driven performance evaluation
- Detailed architecture design based on performance evaluation according to use cases

<table>
<thead>
<tr>
<th>Service Category</th>
<th>Service Description</th>
<th>Item Submitted by Customer</th>
<th>Deliverable from Socionext (Example)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Provide of development environment for advance development of software</td>
<td>A virtual platform for software development is provided</td>
<td>Block diagram</td>
<td>High-speed virtual platform (for software development)</td>
</tr>
<tr>
<td>Provide of environment for software driven performance evaluation</td>
<td>A virtual platform for software driven performance evaluation is provided</td>
<td>Block diagram</td>
<td>High-speed virtual platform (for architecture design)</td>
</tr>
<tr>
<td>Provide of environment for detailed architecture performance evaluation</td>
<td>A virtual platform for architecture performance evaluation is provided. Performance is measured</td>
<td>Architecture construction diagram</td>
<td>High-accuracy virtual platform Performance measurement report</td>
</tr>
</tbody>
</table>

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**Advance development of software**

- Software development

**Software driven performance evaluation**

- Rough architecture design
- Use case extraction

**Architecture performance evaluation**

- Detailed architecture design

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**CPU DMA IP**

**MEM TIM IRC**

**SW**

Determine software architecture, IPs to use, memory mapping, and data flow

**CPU DMA FPGA (RTL)**

**SCEMI-I/F SCEMI-I/F Cross Bar**

**MEM BUS)**

Determine bus width, frequency, bus architecture

**MEM**

**BUS TIM IRC**

Determine detailed configuration, cross-bar and number of FIFO stages.
High level synthesis Support service (Cedar™-HLS)

Cedar™-HLS is a service for mapping from a high-level language (C/SystemC) to our technology. This service reduces the cost and work period for our customers.

**Benefits of high level synthesis**
- Reduced development period: the amount of description is reduced by one tenth and the verification time are reduced by one third (based on our results)
- Reusing of sources: the efficiency of development can be improved (ease of changing devices/technologies)
- Ease of evaluation: performance and footprint (cost) can easily be optimized using parameters

**Example applications of Cedar™-HLS**
- Optimal source code tuning for custom SoCs (source code rewriting)
- Confirmation of high level synthesis results and integrity by performing RTL logic synthesis

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**Cedar™-HLS Service Outline**

**Customer’s tasks**
- Algorithm C/C++
- Specifications, test bench

**Socionext’s tasks**
- Cedar™-HLS service
  - High level synthesis optimization/verification
  - Code, high level synthesis constraints, verification report
  - Performance report option (Timing)

**Provided**
- Library
- RTL Rule Set
- RTL
- RTL Style Check
- Logic synthesis
- Netlist
- Netlist hand-off
- Placement and routing

<table>
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<th>Deliverable from Socionext (Example)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Handing off of RTL designed with high level synthesis RTL hand-off</td>
<td>Rewriting of a language in accordance with the tool Rewriting of a language in accordance with constraints</td>
<td>Functional specifications Constraint conditions High level language</td>
<td>Rewritten high level language Library for high level synthesis RTL designed with high level synthesis</td>
</tr>
<tr>
<td>Handing off of high level language</td>
<td>High level language is handed off and subsequent LSI design is performed under contract</td>
<td>(subject to the above described service)</td>
<td>SoC devices</td>
</tr>
<tr>
<td>Cedar™ coordination</td>
<td>High level synthesis of RTL for FPGA High level synthesis of RTL for ESL</td>
<td>Functional specifications Constraint conditions High level language</td>
<td>RTL SystemC</td>
</tr>
</tbody>
</table>
SoC Logic Design Service

By combining Arm’s CPU and our various functional macros, we offer the best Arm platform for customers’ systems. By suggesting a configuration of CPUs, buses, and memory controllers that takes performance and power into account and measuring performance at an early stage, we provide comprehensive support for custom SoC development.

Customizing verified reference design (SNAP: Socionext Arm Based SoC Platform) allows us to provide high quality platforms in a short time.

SoC Logic Design Outline

Application Example of SoC Logic Design Service

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<tr>
<th>Service Category</th>
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<th>Item Submitted by Customer</th>
<th>Deliverable from Socionext (Example)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SoC Logic Design</td>
<td>Specification design</td>
<td>Requirement specifications, Macros to be installed, Use cases</td>
<td>SoC specifications</td>
</tr>
<tr>
<td></td>
<td>RTL design</td>
<td>Functional and performance requirements</td>
<td>RTL</td>
</tr>
<tr>
<td></td>
<td>RTL verification</td>
<td>Verification specifications, result reports</td>
<td></td>
</tr>
</tbody>
</table>
Custom SoC

High-speed logic verification and power consumption computing service using emulators (Cedar™-EMU)

This design service enables large-scale design to be verified by installing the design of a customer developing a custom SoC on an emulator and accelerating the HDL simulation time by 500 to 1000 times. Since we provide the necessary equipment and operators, the customer only needs to prepare design data and input data to construct an environment.

Example applications of Cedar™-EMU
- System verification of Arm-based image SoCs (ICE debugger can be connected)
- Simultaneous verification of hardware and software linked with ESL
- Functional and performance verification and power consumption analysis of image processing SoCs

Cedar™-EMU Service Outline

We also develop technologies independently and have an option for various pre-silicon analysis.
- Software co-verification: Verification of a system including its software is possible in coordination with a Cedar™-ESL environment
- High accuracy performance display: Cycle accurate detailed performance analysis is possible
- High accuracy power consumption calculation: Power consumption is calculated with cell-level accuracy analysis is possible for each block

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</tr>
</thead>
<tbody>
<tr>
<td>Chip level verification</td>
<td>Formulation of verification specifications</td>
<td>Outline block diagram</td>
<td>Verification specifications</td>
</tr>
<tr>
<td></td>
<td>Creation of verification data</td>
<td>Design data (RTL or netlist)</td>
<td>Verification data</td>
</tr>
<tr>
<td></td>
<td>Construction of verification environment verification</td>
<td>Input/expected value data</td>
<td>Emulation verification results</td>
</tr>
<tr>
<td>System level verification</td>
<td>System level verification using software developed in an ESL environment</td>
<td>Design data (RTL or netlist)</td>
<td>Emulation verification environment</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Input/expected value data</td>
<td>Verification result reports</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Test programs</td>
<td></td>
</tr>
<tr>
<td>Power consumption reduction</td>
<td>Measurement of power consumption</td>
<td>Power measurement program</td>
<td>Reports on results of power consumption measurement</td>
</tr>
</tbody>
</table>
Prototype Board Development Service (Cedar™-PROT)

We provide a prototype board with an FPGA on which custom SoC design is implemented. Since a custom SoC IP is implemented on an FPGA, high equivalence with the custom SoC can be maintained. With the custom SoC IP and user logic implemented on separate FPGAs, this prototype board with a preverified IP allows customers to focus their efforts on the development of a user logic.

Example applications of Cedar™-PROT
- Prototype for system verification
- Prototype for advance development of software

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</thead>
<tbody>
<tr>
<td>System level verification</td>
<td>Provide of a prototype board</td>
<td>Requirement specifications (specified circuit information, etc.)</td>
<td>Board unit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Board specifications</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>FPGA ROM data</td>
</tr>
</tbody>
</table>
PCB Co-design Support Service (PLACATE™)

PLACATE™ is a noise analysis and countermeasure support service based on an integrated LSI and PCB model that greatly supports customers in shortening the system development period and cost reductions through reduced BOM. By applying this service from the upstream phase of custom SoC design and PCB design, we contribute to shortening the design period of customers by reducing the amount of reworking of LSI and PCB design that needs to be done and thereby improving their systems and significantly reducing evaluation workload.

Design Flow Image

Service Description
- Board prototyping
- Wiring/Reducing bypass capacitors
- Integrated noise analysis for LSI, PKG, and Board
- DRAM-IF (DDR4, etc.) Si/PI analysis
- SerDes (PCIe Gen3, etc.) SI analysis
- Creation of LSI power supply models
- LPM+IBIS5.0
- Looking into measures for EMC
- Consulting by INARTE engineers

Deliverable (Example)
- Board design guidelines
- Board reference design
- Si/PI analysis result reports
- LSI power supply model
- LPM+IBIS5.0
- EMI analysis results
- EMI countermeasure proposals

Structure of Simulation Kit

Case of Bypass Capacitor Reduction

Case of EMI Analysis
Software Development Service

This service provides a software platform customized for Arm-SoCs to be developed by customers, based on our system prototyping kit BSP (board support package). Customers can focus their efforts on the development of application software without being bothered by the development of general-purpose functions and shorten the development period of products.

Example of Customization

<table>
<thead>
<tr>
<th>BSP for Socionext’s system prototyping kit</th>
<th>OS porting</th>
<th>Driver customization</th>
<th>Testing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linux, μT-Kernel</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>USB driver, GbE driver, PC/SPI driver</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Socionext’s System Prototyping Board

- Cortex A9/R4F/M3
- USB OTG
- USB 3.0
- GbE

Details of Example Case of Software Platform

<table>
<thead>
<tr>
<th>Application software</th>
</tr>
</thead>
</table>

Software platform

- OS
- Flash NAND driver
- NAND driver
- Console driver
- Standard Lib
- Boot Loader
- USB Class driver
- Protocol driver
- protocol stack driver
- USB driver
- SD driver
- MAC driver
- Encryption driver
- JPEG driver
- PCI driver
- SATA driver
- HDMI driver
- USER circuit driver

Arm core built-in LSI/system board

- Arm core
- SNAP Peripheral
- MEMC
- ROM
- UART
- GPIO
- I2C
- SPI
- USB driver
- SD
- GbE
- Encryption
- JPEG
- PCI
- SATA
- HDMI
- USER circuit

<table>
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<th>Service Description</th>
<th>Item Submitted by Customer</th>
<th>Deliverable from Socionext(Example)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software platform</td>
<td>OS porting, driver customization, testing</td>
<td>Requirement specifications</td>
<td>Implementation specifications, Test specifications and result reports</td>
</tr>
<tr>
<td>OS porting</td>
<td>OS porting, testing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Driver customization</td>
<td>Driver customization, testing</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Provide of Subsystems

Socionext provides subsystems featuring specific functions enabled by combining various types of IP. By incorporating a subsystem, the main system can achieve high performance with a specific function and low power consumption.

Power-saving Subsystems

Background and Initiatives

In step with SoCs getting more functional and highly integrated recently, power consumption also tends to increase. At the same time, due to the restrictions on power consumption, as represented by ErP Lot26, and increasing awareness on energy-saving such as the reduction of CO2 emissions, power-saving is also an important element required for SoCs. Against this background, we have developed a power saving subsystem that satisfies two conflicting elements performance improvement and reduction of power consumption.

Outline

A power-saving sub-system integrates a high performance IP, Arm micro computer, and peripheral I/O. Operating as an always-on block during system standby, the sub-system saves power in terms of the entire SoC by enabling the main system to be stopped completely. During the standby period, the following processing is performed.

- Network standby response such as Ethernet (to be described later)
- Wake-up control based on notification from USB and other interfaces
- Centralized management of power gating and clock gating

Network standby response

Network standby response is a function in which the subsystem carries out packet processing on behalf of the main system when it is in a standby state. This function also supports the following functions.

- Main system wake-up assistance when a packet requiring processing by the main system is received
- The acceleration function that accelerates packet processing in a normal state

Actual Network Standby Response Performance Values

<table>
<thead>
<tr>
<th>Functional/Performance</th>
<th>Normal</th>
<th>When proprietary technology is used</th>
<th>Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stand-by power</td>
<td>≤1.0mW</td>
<td>≤1.0mW</td>
<td>1.0 to 1.0</td>
</tr>
<tr>
<td>Communication performance</td>
<td>300Mbps</td>
<td>900Mbps (20% reduction in CPU load)</td>
<td>Approx. 3 times</td>
</tr>
</tbody>
</table>

Actual measurements on MB86S73 board
Security Subsystem

**Background and Initiatives**

With the recent progress of the IoT (Internet of Things), security functionality is required for various devices. In terms of security functionality, the protection of confidential information stored on network-connected devices and deterrence of unauthorized access or illegal operations are extremely important. Achieving this requires the prevention of software falsification, monitoring by hardware, encryption of the network path, and so on. However, encryption calculation and authentication computing for these security functions impose a very heavy load upon the software. Therefore it is not easy to implement such functionality. To solve this issue, we offer the best subsystem for implementing security functionality.

**Outline**

A subsystem based on Flexware Engine™ realizes various encryption authentication functions. In addition to accelerating general-purpose encryption and authentication processing, the subsystem is capable of accelerating complex processes, such as TLS and IPsec. As high load processes are executed by the dedicated hardware, this subsystem achieves 8 to 16 times higher performance compared to software processing.

**Features**

- Support for various encryption and authentication algorithms (DES/3DES, AES, ARC4, MD5, SHA1/256/512, etc.)
- Diverse hardware offloading and acceleration functions (TCP/IP checksum, TCP segmentation, IPsec frame, TLS record, etc.)
- Support for the connection of Gigabit Ethernet MAC (optional)
- Acceleration of exponentiation, multiplication, division and remainder calculation required for RSA by a public key encryption calculation acceleration macro (F_PKA) (optional)
- The public key encryption calculation acceleration macro (F_PKA) is also available as a stand-alone macro
- Platform (OS) independent SDK

### Supported Algorithms

<table>
<thead>
<tr>
<th>Encryption</th>
<th>IPsec</th>
<th>TLS</th>
<th>Generic</th>
</tr>
</thead>
<tbody>
<tr>
<td>DES-ECB / 3DES-ECB</td>
<td>✗</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>DES-CBC / 3DES-CBC</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>AES-ECB</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>AES-CBC</td>
<td>✓*</td>
<td>✓**</td>
<td>✓**</td>
</tr>
<tr>
<td>AES-CTR</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>ARC4</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>AES-XTS</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>AES-GCM</td>
<td>✓*</td>
<td>✓**</td>
<td>✓**</td>
</tr>
<tr>
<td>AES-XTS</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>AES-XTS</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>AES-XTS</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Authentication</th>
<th>IPsec</th>
<th>TLS</th>
<th>Generic</th>
</tr>
</thead>
<tbody>
<tr>
<td>MD5</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>MD5 (HMAC)</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>SHA1 / SHA256</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>SHA1 / SHA256 (HMAC)</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>SHA512</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>AES-XCBC-MAC-96</td>
<td>✓*</td>
<td>✓**</td>
<td></td>
</tr>
</tbody>
</table>

*1: 128 / 192 / 256 bit
*2: 128 / 256 bit
*3: 128 bit

### Actual Security Subsystem Performance Values

<table>
<thead>
<tr>
<th>Functional</th>
<th>Normal</th>
<th>Sub System</th>
<th>Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLS</td>
<td>14.8Mbps</td>
<td>174Mbps</td>
<td>12 times</td>
</tr>
<tr>
<td>AES-CBC</td>
<td>76Mbps</td>
<td>1250Mbps</td>
<td>16 times</td>
</tr>
<tr>
<td>SHA-1</td>
<td>168Mbps</td>
<td>1380Mbps</td>
<td>8 times</td>
</tr>
</tbody>
</table>

Actual measurements with CAM board
Background and Initiatives

With the spread of the Internet, the need for video streaming is growing. Typical examples are media servers and network monitoring cameras. In such target areas, this subsystem carries out IP packetization of video data, significantly reducing the processing load of the main system.

Outline

Using the Flexware Engine™ as the key part, this subsystem encapsulates video and audio data into an IP packet and encapsulates the IP packet into an Ethernet frame. The following series of processes are performed in the high performance subsystem upon the video data.

- Packetizing video data (ES: elementary stream) into TS packets, if necessary
- Encapsulating ES, TS, or JPEG data into RTP packets
- Encapsulating RTP packets into IP packets
- Encapsulating IP packets into Ethernet frames and performing GMAC control (video transmission)

Features

- Support for RTP/UDP offloading
  - Supported formats
    - ES over RTP : Video (H.264), Audio (G.771, AAC)
    - JPEG over RTP
    - TS over RTP
    - Metadata over RTP
- Support for Max.32 streams
- Integration with security (encryption) functionality
**Video Codec Subsystem**

**Background and Initiatives**
Due to an imbalance between the advance of DDR memory to the ultra-high speed generation along with an increase in the burst length and access by video codec processes handling small size rectangular image data to the DDR, a reduction in the efficiency of using the DDR memory band width has become an issue. This subsystem enables high efficiency video codec processing that can save the band width using Socionext’s unique technology.

**Outline**
We have developed our unique bus protocol methodology that can improve memory access efficiency in the codec process without being significantly affected by advances in DDR. Tightly coupling our codec engine and our memory controller with the methodology enables the memory controller to efficiently access DRAM by taking into account a physical memory map based on the 2D information on image data accessed by the codec engine, reducing the required memory band width significantly.

**Features**
- Achieves HEVC codec processing with a smaller bus width (bit) as listed below.

### Example: When using LPDDR4 2400 Mbps

<table>
<thead>
<tr>
<th></th>
<th>Processing details</th>
<th>Socionext’s conventional system</th>
<th>Video codec subsystem</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>4k 60p 4:2:2 10bit</td>
<td>112bit</td>
<td>64bit</td>
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<td>4k 60p 4:2:0 10bit</td>
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<td>48bit</td>
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<tr>
<td></td>
<td>4k 60p 4:2:0 8bit</td>
<td>64bit</td>
<td>32bit</td>
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<tr>
<td>Encode</td>
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<td>4k 60p 4:2:0 8bit</td>
<td>64bit</td>
<td>32bit</td>
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</table>

### General Relationship between Codec IP Core and DDR Memory

- **Codec engine**
- **Memory controller**
- **DDR memory**
- **General-purpose bus**
- **Bank + Physical address**
- **12 commands**
- **Frequent small memory access**

### Relationship between Socionext Codec IP Core and DDR Memory

- **Codec engine**
- **Socionext’s Codec engine**
- **Memory controller**
- **Socionext’s Memory controller**
- **Logical -> Physical conversion**
- **Bank + Physical address**
- **2 commands**
- **Efficient memory access**

(1) Access with a large rectangular size by taking into account memory access efficiency
(2) Sharing of information on 2D data between the Codec IP and memory controller
Image Signal Processor Subsystem

Background and Initiatives
Under the current circumstances where camera solutions continue to advance, it is extremely difficult to keep providing new functionality and offering differentiating features every year. We have created IP for the image macro part of our image signal processor (Milbeaut®) with a track record of 18 years and provide it as a high-resolution, high-performance subsystem.

Outline
By creating IP for an image macro for each functional block, it is possible to build a flexible platform. Each IP has the AXI interface so SoC integration is easy.

Features
- High-performance 4Kp60 600Mpix/sec (ex TSMC 28nm HPC+)
- API for effectively using image macros is provided.
- An image adjustment simulator is provided to emphasize the individuality of images.

<table>
<thead>
<tr>
<th>IP Block</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>B2B</td>
<td>Bayer domain processing Noise reduction, resizing, defective pixel correction, 3A (AE/AWB/AF) statistics, shading correction</td>
</tr>
<tr>
<td>B2R</td>
<td>Demosaic processing White balance gain, color interpolation</td>
</tr>
<tr>
<td>LTM</td>
<td>Local tone mapping Local tone mapping</td>
</tr>
<tr>
<td>R2Y</td>
<td>RGB to YUV conversion Color correction, tone correction, gamma correction, multi axis color correction, YUV conversion (444/422/420), edge enhancement luminance noise reduction, resizing, Y histogram</td>
</tr>
<tr>
<td>CNR</td>
<td>Color noise reduction Color noise reduction, purple fringing correction</td>
</tr>
<tr>
<td>3DNR</td>
<td>Multi-frame noise reduction Noise reduction with reference to multiple images</td>
</tr>
<tr>
<td>HDR</td>
<td>High dynamic range synthesis Dynamic range expansion by synthesizing two different exposure images</td>
</tr>
<tr>
<td>LDC</td>
<td>Lens distortion correction Correction of image distortion caused by optical characteristics</td>
</tr>
</tbody>
</table>

Low light intensity noise reduction
- 400lux
- 0.01lux

Defective pixel correction

Lens distortion correction
Socionext supports customers with the development of advanced SoC by providing high-quality macros verified by its unique IP macro verification system. We develop our own rich IP lineup, which includes CPU, media processing, image processing, and communication interface, and also prepare various types of IP by cooperating with third-party vendors, to meet a vast range of customer demands with our cutting-edge technologies. We will continue our development focused on the circuit technology expertise cultivated on the high-end platforms, and provide stable and advanced IPs.

As technology advances, system LSIs are increasingly required to have more functions. In response, we have been developing smaller IP macros that consume less power. In addition to reducing power thanks to advances in technology, we provide macros that are available only from Socionext by developing new architectures.
Arm® Solutions

Arm Cores and Design Kits

The comprehensive license agreement with Arm allows customers to select the most suitable Arm core to meet their requirements. We provide the most suitable Arm core and SNAP-DK (design kit), a design environment, for custom SoC for a wide range of applications such as microcontrollers, embedded device, and application equipment.

These Arm Cores in the line-up are available on all process technologies that Socionext offers.

Socionext Arm Platform (SNAP)

Use of the SNAP (Socionext Arm based SoC Platform) reduces development time and risks in Arm core-based SoC development. SNAP consist of the following.

- **Design Kits:** SNAP-DK, ADK, SDK
  - **SNAP-DK**: Consists of an Arm core and minimum required peripheral IPs.
  - **SNAP-ADK**: SNAP-DK-based design kit that already implements an interface macro, GPU, etc.
  - **SNAP-SDK**: This design kit provides a fully customized dedicated subsystem for customers using a design tool in accordance with the requirement specifications.

By selecting the most suitable design kit based on the specifications customers require, development time can be reduced significantly. These design kits, containing a simulation environment, test bench, sample boot code, etc., contribute to the shortening of time to launch the design environment and creation of an appropriate Arm core boot program.

- **Prototyping:** SNAP-PK
  - The SNAP-PK provides Socionext’s unique FPGA board with SNAP-DK. By implementing a user logic on the FPGA side, it achieves prototyping of an SoC.
  - This product can be used for system operation verification of hardware, performance evaluation, and early development of software.

---

**Line-up of Arm Core, GPU and SNAP-DK**

<table>
<thead>
<tr>
<th>Arm core</th>
<th>Available planning</th>
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<td>Arm9</td>
<td>Cortex-R, Cortex-A72, Cortex-A55</td>
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<tr>
<td>Arm7</td>
<td>Cortex-M, Cortex-A53, Cortex-A35</td>
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<table>
<thead>
<tr>
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<td>T820, G71, T620, G51</td>
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<td>DK-11</td>
<td>DK-Av7, DK-Av8, DK-Av8(A53), DK-Av8</td>
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<td>DK-9</td>
<td>DK-Rv7, DK-Rv8</td>
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<td>DK-7</td>
<td>DK-Mv7, DK-Mv8</td>
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</tbody>
</table>

**SNAP Design Kits**

<table>
<thead>
<tr>
<th>Type</th>
<th>Content</th>
<th>Advantage</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNAP-DK (Basic Design Kit)</td>
<td>CPU + small-scale peripheral IPs</td>
<td>Bootable CPU subsystems can be used</td>
</tr>
<tr>
<td>SNAP-ADK (Advanced Design Kit)</td>
<td>SNAP-DK + high performance IPs (system with guaranteed performance)</td>
<td>High performance CPU subsystems including an OS can be used</td>
</tr>
<tr>
<td>SNAP-SDK (System Design Kit)</td>
<td>Consultation-based full custom design kit (system with guaranteed performance)</td>
<td>Dedicated subsystems based on requirement specifications and existing systems can be used</td>
</tr>
</tbody>
</table>

**SNAP-PK**

- Example SNAP-DK-M3
- Customer’s logic
Custom SoC

Socionext provides various DDR interface macros from low-to-middle speed forwarding bandwidth to high-speed forwarding bandwidth or low power, with various process technologies. Moreover, we support development for signal quality and cost optimization through design support by LSI-Package-Board co-design.

DDR interface macros

- High-speed/high-bandwidth DDR3/DDR4
- Low power LPDDR4X/4/3/2 DDR3L
- DFI compliant (all macro)
- Compatible with many different DRAM configurations and PKG options, such as Fly-by, PoP, and DIMM thanks to the PHY function (training function).

DDR Interface Configuration Diagram

- Bus switching verification: Optimizes the write and read bus switch timing

LPDDR4-3733 DQ Waveforms

Bus Switching Waveforms

Driver/OS: SNAP-Linux

SNAP-Linux provides the Linux kernel for which operation has been checked on the SNAP-PK and various IP drivers. This product contributes to reducing software development time for customers.

SNAP (Socionext Arm Platform)

SNAP-Linux provides the Linux kernel for which operation has been checked on the SNAP-PK and various IP drivers. This product contributes to reducing software development time for customers.

Interface Macros

DDR Interface

Socionext provides various DDR interface macros from low-to-middle speed forwarding bandwidth to high-speed forwarding bandwidth or low power, with various process technologies. Moreover, we support development for signal quality and cost optimization through design support by LSI-Package-Board co-design.

- DDR interface macros
  - High-speed/high-bandwidth DDR3/DDR4
  - Low power LPDDR4X/4/3/2 DDR3L
  - DFI compliant (all macro)
  - Compatible with many different DRAM configurations and PKG options, such as Fly-by, PoP, and DIMM thanks to the PHY function (training function).

- DDR interface design support (LSI-Package-Board codesign)
  - Timing verification: Verifies the timing of all DDR-IF systems including delays between LSI I/O and DRAM
  - Power Integrity: Optimizes the parasitic inductance, resonant frequency, and power supply (PKG, PCB) impedance as part of the power supply impedance design
  - Signal Integrity: Optimizes Driver strength, terminator resistance, and interconnect topology

SNAP (Socionext Arm Platform)

SNAP-Linux provides the Linux kernel for which operation has been checked on the SNAP-PK and various IP drivers. This product contributes to reducing software development time for customers.
Memory Controllers

Socionext provides various memory solutions for system optimization. We also offer consulting services on memory systems including memory channels and the system bus to maximize SoC performance.

- **Memory controller IP**
  - Controller for maximizing high DRAM utilization

- **QoS-Arbiter IP**
  - High performance QoS-Arbiter featuring multiple functions

- **BusIP**
  - Original low power consumption bus with high layout flexibility

- **MonitorIP**
  - Visualizes memory system performance in real-time
  - Monitors performance (bandwidth, latency) and provides an environment for tuning parameters

MIPI Interface

This high-speed interface is used to build a camera and display system by combining high-speed, high resolution CMOS image sensors. This interface provides a solution for highly expressive images.

- **MIPI D-PHY TX macro**
  - Small footprint, high-performance macro with the maximum speed of 4.5 Gbps
  - 4-data lane + 1-clock lane configuration
  - Transmission speed: 80 Mbps to 4.5 Gbps per lane
  - Equalization function
  - The world’s smallest footprint
  - D-PHY2.0 compliant
PCI Express Interface

As a result of the recent rapid improvement in CPU processing capability and an increase in the need for high capacity data transfer, it has become extremely difficult to achieve the expected system performance with existing buses. The PCI Express technology is a high-speed interface capable of transferring several hundred megabytes of data that can overcome this issue.

Socionext’s PCI Express macro supports up to 8 GT/s (Gen3) and passed the PCI Express standard compliance test hosted by the Peripheral Component Interconnect Special Interest Group (PCI-SIG), and its interconnectivity and reliability have been confirmed with many PCI Express interfaces.

- **PCI Express LINK macro**
  - Compliant with the PCI Express Base Specification rev.3.0 standard specification
  - Support for x1, x4, and x8 lanes
  - DualMode (RootComplex or Endpoint is selectable)
  - Possible to select AMBA3 I/F as the user interface
  - Built-in DMAC

- **PCI Express PHY macro**
  - Maximum transfer bit rate of 64 GT/s
  - High-speed signal transmission with the de-emphasis function is guaranteed
  - The LINK macro interface is compliant with the PIPE3 and PIPE4 standard specifications
10G-28Gbps SerDes Interface

With transmission performance of 10Gbps–28Gbps per channel and a configuration comprised of multiple channels, we provide a high-performance SerDes macro for constructing 100G/200G/400G optical networks or 100G Ether systems. The built-in low-jitter, high-performance PLL enables robust transmission up to 28 Gbps per channel. It also supports various standards including OIF-CEI-11G-SR, OIF-CEI-28G-SR, OIF-CEI-28G-VSR, IEEE802.3ba CAUI, IEEE802.3bm CAUI4, XFI and so forth.

- ×1, ×4 lane configuration.
- Comprised of Transmitter/Receiver/PLL and capable of bidirectional communication with 1 macro.
- Up to 112.8 Gbps per macro (for unidirectional, ×4 configuration).
- Support for power-down control on each lane.
- Support for power-down control for the entire macro.
- Implementing Clock-Data Recovery for each Receiver lane.
- Transmitter Equalization supported.
- Receiver Equalization supported.
- Built-in termination resistor in Transmitter/Receiver.
- Organic flip chip package.
  (0.8 mm/1.0 mm Ball Pitch, HDBU Package)
**Analog Macros**

We offer various analog macros (data converter, power management, temperature sensor, analog front-end) for our customers’ development to address various applications including communication, image processing, sensors and control.

- All macros are silicon verified.
- Implemented on many custom SoCs with a track record in mass production.

**Data Converters**

We offer various data converter macros addressing low power consumption and a small area which are demanded in SoCs.

- **Pipeline & high speed SAR ADC**
  - 10-bit/12-bit resolution, maximum 200MSPS conversion rates
  - The world’s smallest class power consumption

**Power Management**

We offer various power management macros that enable single power supply development which is demanded in SoCs.

- **DC-DC converter for large current supply applications**
  - Reduced cost achieved by consolidating power-supply IC functions in SoCs
  - 85% power conversion efficiency
  - Safety protection functions such as short-circuit detection implemented

- **LDO for low noise power supply applications**
  - Line-up of small area version such as integrated I/O type
  - Safety protection functions such as short-circuit detection implemented
  - Power supply to analog IPs such as ADC and PLL supported

**ΔΣ ADC**

- Applicable to 16bit to 24bit resolutions
- Power consumption of up to 1 mW with high precision SINAD 85 dB

**ΔΣ DAC**

- Applicable to 16bit to 24bit resolutions
- SINAD 90 dB. Power consumption is 1 mW or less
**Temperature Sensor**

We offer temperature sensor macros for voltage and frequency control according to chip temperature.

- Chip temperature monitoring at a high resolution (0.125°C step) enabled by the built-in high accuracy ADC
- Multiple sensors installed on one chip due to low power consumption and small area

**Analog Front-End (AFE)**

We offer low power consumption AFES for processing various sensor signals.

- **Touch panel AFE**
  - Suitable for 4-wire resistive film touchscreen panels
  - Built-in driver circuit for operating resistive films
  - 12-Bit SAR ADC installed
  - Touch position detection, pen pressure detection and pen interrupt functions supported

- **Scanner AFE**
  - Both CCD and CIS supported
  - Gain and offset adjustment function implemented
  - 12-bit high-speed ADC installed
  - Low power consumption (72mW)

- **Power line communication (PLC) AFE**
  - High-speed PLC standards (HD-PLC, IEEE1901, etc.) compliant
  - High accuracy and high-speed ADC/DAC circuits installed
    - Transmitter : 10-bit 250MSPS 3.3V DAC
    - Receiver : 10-bit 125MSPS 1.2V ADC
  - Low power consumption (365mW)
### Functional/Interface Macros

<table>
<thead>
<tr>
<th>Category</th>
<th>Function</th>
<th>90nm</th>
<th>65nm</th>
<th>55nm</th>
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*: For details, refer to security subsystems on page 15.

### High Speed Interface Macros

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(continued on the following page)
### High Speed Interface Macros

<table>
<thead>
<tr>
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<th>Function</th>
<th>90nm</th>
<th>65nm</th>
<th>55nm</th>
<th>40nm</th>
<th>28nm</th>
<th>16nm/12nm</th>
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<tr>
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<td>DRAM Interface (PHY)</td>
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### Analog Macros

<table>
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<th>Category</th>
<th>Function</th>
<th>90nm</th>
<th>65nm</th>
<th>55nm</th>
<th>40nm</th>
<th>28nm</th>
<th>16nm/12nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>8bit, up to 140MSPS</td>
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<td>✓</td>
<td>✓</td>
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<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>ADC</td>
<td>10bit, up to 200MSPS</td>
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<tr>
<td>ADC</td>
<td>12bit, up to 200MSPS</td>
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<td>✓</td>
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<tr>
<td>ADC</td>
<td>16bit</td>
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<tr>
<td>DAC</td>
<td>10bit, up to 220MSPS</td>
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<tr>
<td>DAC</td>
<td>12bit, up to 110MSPS</td>
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<tr>
<td>DAC</td>
<td>16bit</td>
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<td>✓</td>
<td>✓</td>
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<td>✓</td>
<td>✓</td>
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<tr>
<td>AFE</td>
<td>Audio</td>
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<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
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<tr>
<td>AFE</td>
<td>Video</td>
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<tr>
<td>AFE</td>
<td>Touch Panel</td>
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<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Temperature sensor</td>
<td>+/-5deg.C accuracy (without trimming)</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Regulator</td>
<td>Vin=3.3V, Vout=1.0-1.2V, Iout≤200mA LDO</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
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<td>✓</td>
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<tr>
<td>Regulator</td>
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</tr>
<tr>
<td>Standard PLL</td>
<td>Fout: ~1200MHz, Fin:10–200MHz</td>
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<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Standard PLL</td>
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<tr>
<td>Standard PLL</td>
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<tr>
<td>Low Jitter PLL</td>
<td>Fout: ~600MHz, Fin:11–100MHz</td>
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<tr>
<td>Low Jitter PLL</td>
<td>Fout: ~6000MHz, Fin:20–100MHz</td>
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<tr>
<td>Fractional -N PLL</td>
<td>Fout: ~1600MHz, Fin:10–50MHz</td>
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<td>✓</td>
<td>✓</td>
<td>✓</td>
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<tr>
<td>Fractional -N PLL</td>
<td>Fout: ~3200MHz, Fin:10–50MHz</td>
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<tr>
<td>SSCG</td>
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<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>SSCG</td>
<td>Fout: ~3200MHz, Fin:10–50MHz</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
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</tr>
</tbody>
</table>
Advanced Front-end and Back-end Design Techniques

**Design Methodology**

As LSIs become more refined, the number of gates that can be mounted is increasing. In custom SoC development, the demand for chip designs with more than 100-million gates is increasing. It is also becoming important to fulfill the demands of more complicated designs such as reduction of power consumption. In these circumstances, Socionext supports customers in developing LSIs by providing the best design environment needed for each technology.

![Diagram](image)

### User Interface

We provide the three types of basic design interfaces shown below as selectable design methodologies. The optimal combination of customers’ design assets and our design technologies and assets improves the efficiency of SoC development projects. We also provide a design flow that incorporates upstream verification and FPGA prototyping, supporting ever higher quality projects and shorter development periods.

### Three Types of Development Interface

<table>
<thead>
<tr>
<th>: Customer</th>
<th>Case1</th>
<th>Case2</th>
<th>Case3</th>
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</thead>
<tbody>
<tr>
<td>Specification</td>
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<tr>
<td>Logic design</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Logic synthesis</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Physical design</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Manufacture</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Testing</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sample shipment</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Development support service (DesignExpress™)**

- User interface: Best combination of customer’s assets and Socionext’s design technologies/assets
- Successful project
- Chip-package co-design: Prototyping of chip and package

**LSI design flow**

- Best design environment supporting advanced technologies

**Back-end design**

- Physical aware logic synthesis
- Optimization that takes into account multiple modes and corners
- Power rail analysis/crosstalk noise analysis

**Low power consumption technology**

- Multiple power supply/multiple voltage design
- Clock gating
- Power management
- Adaptive power supply control (AVS*/Advanced-AVS)
- Standard cell
- Low power SRAM
- Low power consumption design environment fully adopting UPF/CPF
- At-speed and low power test technologies
- Memory redundancy repair process and fault diagnosis technologies

**Advanced Front-end and Back-end Design Techniques**

- High level synthesis
- Front-end design kits
- Multiple power supply/multiple voltage design
- Physical aware logic synthesis
- Optimization that takes into account multiple modes and corners
- Power rail analysis/crosstalk noise analysis
- Multiple power supply/multiple voltage design
- Clock gating
- Power management
- Adaptive power supply control (AVS*/Advanced-AVS)
- Standard cell
- Low power SRAM
- Low power consumption design environment fully adopting UPF/CPF
- At-speed and low power test technologies
- Memory redundancy repair process and fault diagnosis technologies
We apply an optimized flow based on the following design flow to suit the characteristics of the LSI being developed.

Outline flow of LSI design

System level design
- System specification design
  - System level design

Front-end design
- RTL design (high level synthesis)
  - Functional verification
  - Initial logic synthesis
    - Initial floor planning
      - physical aware
        - logic synthesis
          - Equivalence verification
            - Timing constraint verification
              - Handoff verification

Back-end design
- Design planning
  - Layout placement and routing
    - Variation considered timing analysis
      - Crosstalk noise analysis
        - Power rail analysis
          - Sign-off verification

Design planning
- Inserting test circuit
  - DFT
    - Test pattern generation

Physical design
- Sign-off verification
  - Physical verification
    - Litho verification
  - Gate simulation
    - Power consumption
      - analysis
Front-end Design

Front-end Design kit

We offer a development environment using standard EDA tools as a SoC development environment for customers and a tool we created for improving design efficiency as a design kit. The front-end design kit, which is uniquely optimized by Socionext, enables the development of high performance, small chip size, low power LSIs.

EDA tools supported by Socionext front-end design kit

<table>
<thead>
<tr>
<th>EDA tool</th>
<th>Cadence, Inc.</th>
<th>Synopsys, Inc.</th>
<th>Mentor Graphics Co.</th>
<th>We provide a checker we developed in-house to suit the technology.</th>
</tr>
</thead>
<tbody>
<tr>
<td>High level synthesis</td>
<td>Catapult<em>2, C-to-Silicon Compiler</em>1, Stratus*1</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>RTL style check</td>
<td>SpyGlass*2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Functional verification</td>
<td>Verilog-HDL Incise Enterprise Simulator<em>1, Questa</em>2, VCS-MX, VCS*2</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>VHDL</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CPF/UPF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic synthesis</td>
<td>Design Compiler<em>2, Encounter RTL Compiler</em>1, Genus Synthesis Solution*1</td>
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<tr>
<td>Equivalence verification</td>
<td>Encounter Conformal Equivalence Checker<em>1, Formality</em>2</td>
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<td>Timing constraint verification</td>
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<td>Encounter Conformal Lowpower<em>1, VC Static Low Power</em>2</td>
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<td></td>
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<tr>
<td>Analysis/debugger</td>
<td>Verdi*2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pre-DFT check*</td>
<td>SpyGlass*2</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

High level Synthesis

As chips becomes larger in scale and more complicated, the design environment customers use is also advancing from conventional RTL design to system level design and verification using higher abstraction languages (C++/SystemC). Under these circumstances, it has become common to perform high level synthesis from a high abstraction model to RTL for shorter TAT in RTL design. Socionext provides technology libraries optimized for each high level synthesis tool and documentation describing optimization settings to generate appropriate RTL for our technology and design flow in such high level synthesis.
SoC testing is becoming more complicated as processes become more refined, circuit scale increases, circuit operation becomes faster, and much less power is consumed. To resolve this issue, in addition to compressed scan, memory BIST, and boundary scan DFT, we perform high quality testing using various types of DFT technology for improved test quality and yield.

[DFT Technologies Adopted by Socionext]

- **At-speed and low power test technologies for improved test quality**
  - Test using on-chip PLL clocks
  - Test that controls power consumption during testing
- **Memory redundancy repair process and fault diagnosis technologies for improved yield**

![Diagram showing DFT technologies with labels: Boundary scan, IO, Memory BIST, Memory, OCC, Compressed scan, PLL, Logic.]

- **Yield improvement technology:** Memory redundancy relieving process can be performed.
- **Low power test technology:** Test that controls power consumption during testing is supported.
- **At-speed test technology:** Test using on-chip PLL clocks is supported.
Back-end Design

We layout customer design with our high-accuracy analysis technology, high performance synthesis, placement, routing, and high speed technology, and low noise design technology.

- Physical aware logic synthesis
  Due to the increase in circuit size and routing load caused by the progress of refinement, the gap between the estimate at the time of logic synthesis and layout is widening. At Socionext, we minimize the gap with the layout by taking into account layout information from the logic synthesis step. This allows for early confirmation of timing convergence, thereby shortening the development period.

- UPF and CPF support
  We support UPF and CPF and perform physical design and physical verification based on power supply specifications for which functional verification is conducted. This enables high design quality to be achieved even for complex low power consumption technologies.

- Multiple mode/corner-aware optimization
  As refinement progresses, the processes, voltage, and temperature conditions (corner conditions) that should be taken into account are increasing. In addition, the number of operation modes is increasing to enhance multifunctionality and secure the reliability of LSIs. In our physical design, placement, routing, and optimization that take into account multiple corner conditions and operation modes are performed. This makes it possible to reduce the iteration of timing optimization due to conflicts between different corners and modes, which shortens the development period.

- Power rail analysis/crosstalk noise analysis
  As refinement progresses and voltages become lower, the delay variation due to an IR drop (voltage drop) in LSIs and crosstalk noise increases. Through high accuracy IR drop and crosstalk noise analysis, we have verified that they do not affect system operations.
The demand for reducing the power consumption of LSIs has been getting stronger in recent years. In our SoC design efforts, we are undertaking various initiatives to meet customers’ demands for lower power consumption. In order to achieve low power consumption LSIs, it is effective to combine various kinds of technologies as well as using individual technologies. Socionext’s design environment “Reference Design Flow” supports various low power consumption technologies and enables the power consumption of LSIs to be reduced during both operation and standby. By controlling the power supply in particular, we develop methodologies for systematically achieving low power consumption. Also, by fully adopting UPF/CPF, we make low power consumption design easy for customers while minimizing changes to their design assets. The use of UPF/CPF allows for high reliability designs even with low power consumption technology, which it has been extremely difficult to verify in the past.

- **Multi voltage design**
  With this technology, different voltages are supplied to an LSI to reduce power consumption during the operation of circuit blocks for a high-speed operation circuit block, a high voltage is supplied, and for a low-speed operation circuit block, a low voltage is supplied. Using UPF/CPF allows physical design and verification of circuit blocks with different voltages to be performed together, minimizing extension of the development period for low power consumption design.

- **Clock gating**
  Clock gating enables the power consumption of LSIs during operation to be reduced by stopping the supply of clock signals to circuit blocks that do not need to operate.

- **Power management**
  We provide power management technology to control power gating, SRAM sleep, and shut-down mode in a comprehensive manner. By thoroughly eliminating useless, this technology contributes to low power consumption. With its unique power switch controlling system, Socionext’s power management technology suppresses the rush current noise generated when the power supply is turned on and off to prevent LSIs from malfunctioning. In addition, using UPF/CPF allows physical design and verification of circuit blocks that have a power shutdown circuit to be performed together, minimizing extension of the development period.

- **Adaptive power supply control**  
  (DVFS*, AVS/A-AVS)
  We can use DVFS, which is for varying the voltage and frequency according to the required throughput.
This technology also adaptively determines the operating voltage according to voltage variation due to manufacturing variability and operates the LSI at the lowest voltage at which its operation is guaranteed, leading to reduced power consumption of the LSI during both operation and standby.

\*1: DVFS (Dynamic Voltage Frequency Scaling)  
\*2: AVS (Adaptive Voltage Scaling)

### Standard cell

In the area of advanced technology, in addition to the standard cell area, routability contributes to the low power consumption of LSIs. We provide our original standard cell that is far superior to that of other companies. In addition, we offer a rich line-up of cells that are effective for achieving low power consumption of the clock system.

### Low power SRAM

An LSI with high-capacity SRAM may have a problem with the power consumption of the SRAM macro. In such cases, power consumption may be reduced by using a multi-mode SRAM. Multi-mode SRAM features a standby mode, sleep mode, and shut-down mode, as well as a normal operation mode. The standby mode allows for the operating power of an SRAM macro to be 0 by stopping the clock operation inside the macro. In sleep mode, leakage power is reduced by deactivating peripheral circuits of the SRAM macro. Power can only be shut down with an SRAM in shutdown mode. The optimization of the SRAM configuration to be used contributes to low power consumption as well. We help customers select the best SRAM from the logic design phase.

<table>
<thead>
<tr>
<th>Operating Mode</th>
<th>Function</th>
<th>Effect</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal</td>
<td>To operate RAM normally</td>
<td></td>
</tr>
<tr>
<td>Standby</td>
<td>To stop the SRAM operation</td>
<td>The operating power is 0</td>
</tr>
<tr>
<td>Sleep</td>
<td>To retain data</td>
<td>Leakage power is reduced to one-third*1</td>
</tr>
<tr>
<td>Shutdown</td>
<td>To shut down the power with only the SRAM</td>
<td>Leakage power is reduced to one-sixth*2</td>
</tr>
</tbody>
</table>

*: Depends on the SRAM structure

### Low power design environment that fully adopts UPF/CPF

Socionext offers a total solution that supports power gating, multi power supply, and multi-voltage design through consistent power supply specification management with UPF\*1 and CPF\*2. RTL simulation for complicated power supply design due to an increased number of integrated IPs, multi power supply verification, and physical design. This solution allows power shutdown verification to be performed based on RTL simulation by managing power supply specifications as separate logical and physical specifications and defining only the logical specification. Verified RTL and the logical specification for the power supply are handed off to physical design, the power supply physical specification that defines the power supply connection is prepared, and then physical design is performed based on these power supply specifications (UPF/CPF). Managing the power supply specification with UPF/CPF in this way and using it through a design flow clarifies the power supply specification and allows for high reliability design.

\*1: UPF (Unified Power Format) is a standard specification that defines the Low power design guidelines standardized as IEEE Std.1801. (http://www.ieee.org/)  
\*2: CPF (Common Power Format) is a standard specification that defines the Low power design guidelines standardized as Si2. (http://www.si2.org/?page=811)
Chips designed with noise in mind, packages, and PCB co-design

Socionext achieves perfect operation on the first attempt through LSI development based on the chip, package, and PCB codesign flow. While offering a good forecast for design through reference design, we develop and improve LSI models (IBIS, timing model, LSI power supply model) necessary for transmission line analysis of DDR4 and other memory interfaces and USB3.0 and other SerDes interfaces to achieve total optimization in each phase of design based on integrated chips, packages, and PCB analysis. This allows for an issue that used to only be discovered in the actual design phase to be addressed in the prototyping phase.

We offer customers IBIS and a timing model early on in the design stage so that they can conduct transmission line analysis taking timing into account.

The use of IBIS5.0 and an LSI power supply model (chip and package) for PCB power supply impedance analysis and SSO noise analysis allows customers to perform high accuracy development in a short TAT.
Advanced Device Implementation and Manufacturing

Technologies and Device Products

Our device products from 90 nm to 12 nm include standard cell types supporting a wide range of technologies. Socionext is working with multiple foundry partners. Thanks to the synergy effect of their manufacturing capability and the quality control system and design engineering ability of Socionext, we will continue to lead the LSI industry in design and manufacture of cutting-edge custom SoCs.

Standard cell

<table>
<thead>
<tr>
<th>Technology</th>
<th>Series</th>
<th>Power Supply Voltage (Typ.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 nm FinFET CMOS</td>
<td>T.B.D.</td>
<td>T.B.D</td>
</tr>
<tr>
<td>12 nm FinFET CMOS</td>
<td>CS661 series</td>
<td>+0.7V ±0.07V / +0.8V ±0.08V</td>
</tr>
<tr>
<td>16 nm FinFET CMOS</td>
<td>CS602 series</td>
<td>+0.7V ±0.07V / +0.8V ±0.08V</td>
</tr>
<tr>
<td>28 nm Metal Gate CMOS</td>
<td>CS407 series</td>
<td>+0.8V ±0.08V / +0.9V ±0.09V</td>
</tr>
<tr>
<td>28 nm Metal Gate CMOS</td>
<td>CS405 series</td>
<td>+0.9V ±0.09V</td>
</tr>
<tr>
<td>40 nm Si Gate CMOS</td>
<td>CS302 series</td>
<td>+1.1V ±0.1V</td>
</tr>
<tr>
<td>55 nm Si Gate CMOS</td>
<td>CS251 series</td>
<td>+1.2V ±0.1V</td>
</tr>
<tr>
<td>65 nm Si Gate CMOS</td>
<td>CS201 series</td>
<td>+0.9 V to +1.3 V (supports a wide range)</td>
</tr>
<tr>
<td>90 nm Si Gate CMOS</td>
<td>CS101 series</td>
<td>+0.9 V to +1.3 V (supports a wide range)</td>
</tr>
</tbody>
</table>

Gate scale comparison

Power consumption comparison

*1: The vertical axis shows the relative ratio of each technology using the total power (sum of the dynamic component and leakage component) of CS101 as the criterion.
Advanced Packages

Package System

From high performance models for high end use to high cost performance models for consumer use, we provide a wide range of packages.

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Package Structure</th>
<th>Thermal Resistor $\Theta ja^*$ (°C/W)</th>
<th>Example Purposes</th>
</tr>
</thead>
<tbody>
<tr>
<td>FC-CBGA</td>
<td></td>
<td>7~</td>
<td>Servers, high-speed large capacity network, etc.</td>
</tr>
<tr>
<td>FC-PBGA</td>
<td></td>
<td>7~</td>
<td>Factory automation, office equipment, medical care, health care, satellite broadcasting, digital TVs, set-top boxes, digital signage, etc.</td>
</tr>
<tr>
<td>FC-PBGA (Conventional)</td>
<td></td>
<td>9~</td>
<td></td>
</tr>
<tr>
<td>TEBGA</td>
<td></td>
<td>13~</td>
<td></td>
</tr>
<tr>
<td>PBGA</td>
<td></td>
<td>15~</td>
<td></td>
</tr>
<tr>
<td>FBGA</td>
<td></td>
<td>17~ to 60</td>
<td>Mobile devices, digital still cameras, camcorders, action cameras, drones, security devices, wearable devices, etc.</td>
</tr>
<tr>
<td>FCCSP</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>QFN</td>
<td></td>
<td>20~ to 40</td>
<td></td>
</tr>
<tr>
<td>WL-CSP</td>
<td></td>
<td>25~ to 60</td>
<td></td>
</tr>
<tr>
<td>LQFP/TEQFP</td>
<td></td>
<td>15~ to 100</td>
<td></td>
</tr>
</tbody>
</table>

*1: Reference value. The thermal resistance value varies depending on the chip size or package specification. Inquire to us regarding individual cases.

Package Roadmap

Through a strong partnership with outsource assembly and test (OSAT) in Japan and overseas, we provide packages with well balanced technology, cost, quality, and reliability.
Simulation

Utilizing advanced simulation technologies, we offer the best package solution.

● Mechanism simulation
Incorporating mechanism simulation into package design allows customers to propose high reliability packages.

● Thermal design simulation
By combining actual measurement of thermal resistors and thermofluid simulation, we perform high accuracy thermal resistance analysis reproducing the operating environment of products.

● Thermal resistance measurements
Measurement of transient thermal resistance values in accordance with the JEDEC standard JESD51-14 is possible.
The products of Socionext are utilized in various fields and are playing very important roles in our customers’ products. We build quality products that meet the varying QCD (Quality, Cost, and Delivery) needs of our customers. Additionally, through comprehensive management systems for the planning and design stages, we as a fabless company choose perfect partner companies (contract manufacturers) in Japan and overseas according to the characteristics, functionality, and quality of products to be manufactured. Moreover, by leveraging our high-quality and reliable technology that has been developed in the global market and through strong cooperation with our partner companies (contract manufacturers), we provide optimum quality to our customers in a timely manner.

Selecting a foundry is a critical part of ensuring optimum quality. In Socionext, we coordinate with domestic and overseas foundry partners that have state-of-the-art technologies and have established an advanced quality assurance system in order to provide the best solutions to satisfy the diverse needs of our customers.

ISO9001 is an international standard for quality management systems with the aim of improving product quality assurance systems and increasing customer satisfaction. We acquired ISO9001 certification. Furthermore, we have set up a system that can expand globally using the production lines of partner companies that have the ISO/TS16949 certification, which is standard in the automotive industry.
Socionext Inc.
Nomura Shin-Yokohama Bldg., 2-10-23 Shin-Yokohama,
Kohoku-ku, Yokohama, Kanagawa, 222-0033, Japan
Tel. +81-45-568-1015
http://socionext.com/en/

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