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Preliminary Data Sheet

SC1701BK3-200
SC1701BH5-200
SC1701BH5-300

Rev0.75 | September 23, 2020

Socionext Europe GmbH

Graphic Competence Center – GCC

Attached Files

Preface

Intention and Target Audience of this Document

This document describes and gives you detailed insight to the stated Socionext Europe GmbH product.

The SC1701 family devices belong to the SoC Family used for graphics applications.

This document is intended for engineers developing products that use the SC1701BK3-200 or SC1701BH5-200 devices. The document describes the function and operation of the devices. Please read this document carefully.

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History

Revision	Date	Description
0.01	10.04.2018	First release - for review
0.10	02.05.2018	First preliminary release
0.15	12.07.2018	1. Overview: updated “1.3.2. Video-Related Features”: Max pixel clock 2. Electrical Characteristics: added “Figure 2.3. : Power-On Sequence”
0.16	28.09.2018	1. Overview: updated SRAM feature in System Features. 2. Electrical Characteristics: Updated notes in Table 2.5, “Clock Input Specifications”, added Section “2.7. Flash Memory Program / Erase Characteristics”.
0.25	09.11.2018	Updated attached files. 1. Overview: updated“1.2. Features”, “1.3. Device Comparison”, “1.4. Block Diagrams”, “1.7.2. SC1701BH5-200/300 Pin Overview”.
0.30	08.03.2019	Throughout document changed SC1701A... → SC1701B... 1. Overview: Added Test section to “1.2. Features” and section “1.6. Part Number Code”. 2. Electrical Characteristics: Updated “2.5. Reset Timing” and “2.9.2. Configuration Pins”.
0.40	22.07.2019	Updated attached pinlists to rev1.21. 1. Overview: Removed “On chip power on reset” from “System Features”; updated “1.4. Block Diagrams”. 2. Electrical Characteristics: Updated “2.2. Power Consumption”; removed On-Chip Power On reset (POR) Characteristics; added “2.8. ADC Sampling Time”.
0.50	31.03.2020	Throughout manual: Added new variant SC1701BH5-300 and its relevant information. Removed MIPI and VESA DSC (Display Stream Compression Decoder) information, will not be supported. Attachments: Added attachment Pinmux_MII_RMII.xlsx. Updated pinlists to version 1.22. Pinout version renamed to 1.22. 1. Overview: Added specifications for SC1701BH5-300. Updated “1.2. Features”; Video Input Interfaces Table 1.5 , Table 1.6 ; “1.3. Device Comparison”; “1.4. Block Diagrams”;“1.7.2. SC1701BH5-200/300 Pin Overview”. 7. Electrical Characteristics: Added Junction temperature (Tj) values to Table 2.2, “Recommended Operating Conditions”; “2.3. Thermal Design Considerations”; “2.10.9. RMII Interface”. Updated “2.6. Power-On Sequence”; “2.10.8. MII Interface”; “2.8.1. ADC Electrical Characteristics”; Table 2.24, “IO circuit types” see VOS values for RSDS, LVDS, and miniLVDS.
0.60	11.05.2020	Attachments: Updated SC1701BH5-300 pinlist to rev1.23. DISP1 or DISP0 now supported in SC1701BH5-300. 2. Electrical Characteristics: Added Junction Temp. (TJ) and OSC values to Table 2.1, “Absolute Maximum Ratings”; “2.3. Thermal Design Considerations”; “2.10.9. RMII Interface”. Updated “2.1.2. Recommended Operating Conditions”; “2.2. Power Consumption”; “2.6. Power-On Sequence”; Figure 2.4, “ADC input signal; “2.10.8. MII Interface”; Table 2.24 .
0.70	30.07.2020	1. Overview: Updated Table 1.1, “Overview of SC1701 Series”, and “1.6. Part Number Code”. 2. Electrical Characteristics: Updated “2.10.3.3. LVDS Mode”. Restructured “2.11. IO Circuit Types” and updated all “2.11.6. MSIO (Multi Standard IO)” circuits.
0.75	23.09.2020	1. Overview: Added details to SC1701-BK3 Package figure

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1. Overview

This document describes the features and functions of the SC1701 family devices SC1701BK3-200, SC1701BH5-200 and SC1701BH5-300.

Note: The content of this document is subject to minor changes. Please check the "History" page for a record of the latest updates and modifications.

Table 1.1. : Overview of SC1701 Series

Device type	Variants and differentiation
SC1701BK3	SC1701BK3-100: Fully featured device. SC1701BK3-10N: No HDCP functionality at APIX link. SC1701BK3-200: No APIX or HDCP functionality.
SC1701BH5	SC1701BH5-100: Fully featured device. SC1701BH5-10N: No HDCP functionality at APIX link. SC1701BH5-200: No APIX or HDCP functionality. SC1701BH5-300: No APIX or HDCP functionality, no mini-LVDS output.
Note: ES1 (Engineering Sample 1) refers to SC1701AK3 and SC1701AH5 devices. For a breakdown of the part number code see "1.6. Part Number Code".	

1.1. General

The SC1701 devices are state-of-the-art graphics controllers especially designed for remote display applications in the automotive industry.

The target application areas are dashboard displays, HUD (Head-Up Display) systems, CID (Central Information Displays) and any other display systems within a car.

1.2. Features

The SC1701 devices are system-on-chip solutions for graphics applications which incorporate graphics engines and graphics display controllers. The features of the SC1701BK3-200 and SC1701BH5-200/300 devices are listed below.

Technology

- CMOS 55nm NVM
- Power supply voltages:
  - 3.3V IO supply
  - 1.2V core supply

Temperature Range

- T_a= -40...105°C

Package

- SC1701BK3-200: HS-BGA-319
  - 23x23mm
  - 1.0mm ball pitch
- SC1701BH5-200/300: EP-LQFP-216
  - 24x24mm
  - 0.4mm pin pitch

Clock Generation

- On-chip oscillator (with external 30.0MHz crystal, 100ppm accuracy)
- On-Chip low-jitter 1.5GHz video PLL for each pixel pipeline and each LVDS capture input (overall: 4 instances of video PLL)

System Features

- SC1701BK3-200: 2 display support
- SC1701BH5-200/300: 1 display support
- SC1701BK3-200: 300MHz system clock
- SC1701BH5-200/300: 200MHz system clock
- 128kB embedded FLASH memory with ECC
- 256kB embedded SRAM video memory
- 9kB embedded SRAM with ECC (1kB freely usable, 8kB used by internal modules like Command Sequencer)
- Embedded programmable core (Command Sequencer, 2 cores)
- DMA controller
- Touch controller support (hardware accelerated communication with external touch devices)
- Configuration FIFO (to decouple host command stream and generate isochronous reconfiguration with internal peripherals)
- High-speed quad-mode SPI to connect external Flash or RAM devices
- Spread Spectrum Clock Modulation (for pixel clocks and system clock)
- Watchdog, Alive sender
- CRC checksum calculation unit for checking of memory content
- PVT monitor
- Configuration interfaces
  - Host SPI configuration interface
  - Ethernet controller (thru ext-PHY)

High-speed interfaces for video streams

- SC1701BK3-200
  - 2x RX LVDS single mode
  - 1x RX LVDS dual mode
  - 1x TX RSDS single/dual mode
  - 2x TX LVDS single/dual mode
  - 2x TX miniLVDS 3/6 pair mode

- 1x TX LVDS quad mode

- SC1701BH5-200/300
  - 1x RX LVDS single mode
  - 1x RX LVDS dual mode
  - 1x TX RSDS single mode
  - 1x TX LVDS single/dual mode
  - 1x TX miniLVDS 3/6 pair mode (only in SC170BH5-200)

SEERIS MVL3 graphics features

- SC1701BK3-200: 2 display controllers (display output)
- SC1701BH5-200/300: 1 display controller (display output)
  - For each display controller:
    - Up to 30bit color resolution
    - SC1701BK3-200: Up to 266Mpix/s in single (533Mpix/s in dual) display controller mode
    - SC1701BH5-200: Up to 160Mpix/s (only single display controller mode)
    - SC1701BH5-300: Up to 140Mpix/s (only single display controller mode)
    - Timing controller with up to 12 signal generators
    - Safety display layer for critical content
    - Signature unit (up to 16 windows / 8 in SC1701BH5-300)
    - IDHash unit (up to 4 windows per pipeline)
    - Dithering, Matrix and Gamma units
- SC1701BK3-200: 2 capture controllers (video input)
- SC1701BH5-200/300: 1 capture controller
  - For each capture controller:
    - Video timing analyzer
    - Histogram measurement
    - Test image generator
    - Line splitter (not supported in SC1701BH5-300)
    - Upscaling/Downscaling (not supported in SC1701BH5-300)
- Memory stream
  - Safety layer/memory layer inside
  - Boot-logo or default stream
  - Debug overlay

Peripherals

Note: Peripherals share pins; the following list represents the maximum number of available peripherals.

- 6x stepper motor controller (3.3V)
- 2x I^2C + slave function
- 4x SPI (shared with one HS-SPI)
- 2x HS-SPI
- 2x USART/LIN
- SC1701BK3-200: 10-channel ADC
- SC1701BH5-200/300: 8-channel ADC
- 16x PWM
- SC1701BK3-200: Max 139 GPIO
- SC1701BH5-200/300: Max 133 GPIO
- CRC unit
- Ethernet arbiter
- I^2S
- Sound generator
- Memory and peripheral protection units
- 8 external interrupts
- 16 reload timers
- CAN in Listen-Only mode

Diagnostics

- Failure unit
  - Panic switch
  - Alive sender
  - System watchdog
- CRC unit
- FLASH with ECC
- SRAM with ECC
- Privileged Access
- Test Register
- HW analysis support for video freeze detection (evaluation cluster)
- Video signature unit (8 per display output)

Test

- Support for boundary scan (IEEE 1149.1-2001)

Display Interfaces

Table 1.2. : SC1701BK3-200 Display Interfaces

#	Interface	Color depth	#Pins	TCON	Max Pin Freq.	Max Pix Freq.(*1)	Example resolution(*4)
2x	LVDS single mode(*2)	18bit	4x2 Diff	External	1050Mbit/s	150Mpix	~1920x1080
		24bit	5x2 Diff				
		30bit	6x2 Diff				
2x	LVDS dual mode(*2)	18bit	8x2 Diff	External	1050Mbit/s	300Mpix(*3)	~2560x1600@60Hz (>270Mpix) ~2880x1080@60Hz (>205Mpix/s)
		24bit	10x2 Diff				
		30bit	12x2 Diff				
1x	LVDS quad mode(*2)	18bit	16x2 Diff	External	1050Mbit/s	533Mpix	~3840x2160@60Hz
		24bit	20x2 Diff				
		30bit	24x2 Diff				
2x	Mini LVDS 3 pair(*2)	18bit	8x2 Diff Up to 12 CMOS	Internal	450Mbit/s	150Mpix	~1920x1080
		24bit			600Mbit/s		
2x	Mini LVDS 6 pair(*2)	18bit	14x2 Diff + Up to 12 CMOS	Internal	450Mbit/s	300Mpix	~2560x1600@60Hz (>270Mpix) ~2880x1080@60Hz (>205Mpix/s)
		24bit			600Mbit/s		
1x	RGB(*2)	18bit	18 CMOS 4 CMOS	External	85Mbit/s Data 170Mbit/s Clk	85Mpix	~1440x900
1x	RSDS single mode(*2)	18bit	10x2 Diff +12 CMOS	Internal	170Mbit/s	85Mpix	~1440x900
		24bit	13x2 Diff +12 CMOS				
		30bit	16x2 Diff +12 CMOS				
1x	RSDS dual mode(*2)	18bit	20x2 Diff +12 CMOS	Internal	144Mbit/s	144Mpix	~1920x1080 (RB), 1220x720 (90Mpix)
		24bit	26x2 Diff +12 CMOS				
		30bit	32x2 Diff +12 CMOS				

(*1) Speed applies to panel interface only.

(*2) Shared multi-standard IO cell is used.

(*3) Two pixel pipelines needed to transport 2x150Mpix/s.

(*4) These are only example resolutions. Maximum resolutions are determined by the maximum pixel frequencies.

RB: Reduced blanking

Table 1.3. : SC1701BH5-200 Display Interfaces

#	Interface	Color depth	#Pins	TCON	Max Pin Freq.	Max Pix Freq.(*1)	Example resolution(*3)
1x	LVDS single mode(*2)	18bit	4x2 Diff	External	800Mbit/s	114Mpix/s	~1920x720
		24bit	5x2 Diff				
		30bit	6x2 Diff				
1x	LVDS dual mode(*2)	18bit	8x2 Diff	External	600Mbit/s	160Mpix/s	~1920x1200
		24bit	10x2 Diff				
		30bit	12x2 Diff				
1x	Mini LVDS 3 pair(*2)	18bit	8x2 Diff Up to 12 CMOS	Internal	450Mbit/s	150Mpix/s	~1920x1080
		24bit			600Mbit/s		
1x	Mini LVDS 6 pair(*2)	18bit	14x2 Diff + Up to 12 CMOS	Internal	450Mbit/s	160Mpix/s	~1920x1080
		24bit			600Mbit/s		
1x	RGB(*2)	18bit	18 CMOS 4 CMOS	External	85Mbit/s Data 170Mbit/s Clk	85Mpix/s	~1440x900
1x	RSDS single mode(*2)	18bit	10x2 Diff +12 CMOS	Internal	170Mbit/s	85Mpix/s	~1440x900
		24bit	13x2 Diff +12 CMOS				
		30bit	16x2 Diff +12 CMOS				

(*1) Speed applies to panel interface only.

(*2) Shared multi-standard IO cell is used.

(*3) These are only example resolutions. Maximum resolutions are determined by the maximum pixel frequencies.

Table 1.4. : SC1701BH5-300 Display interfaces

#	Interface	Color depth	#Pins	TCON	Max Pin Freq.	Max Pix Freq.(*1)	Example resolution(*3)
1x	LVDS single mode(*2)	18bit	4x2 Diff	External	800Mbit/s	114Mpix/s	~1920x720
		24bit	5x2 Diff				
		30bit	6x2 Diff				
1x	LVDS dual mode(*2)	18bit	8x2 Diff	External	500Mbit/s	140Mpix/s	~1920x1080 (RB)
		24bit	10x2 Diff				
		30bit	12x2 Diff				
1x	RGB(*2)	18bit	18 CMOS 4 CMOS	External	85Mbit/s Data 170Mbit/s Clk	85Mpix/s	~1440x900
1x	RSDS single mode(*2)	18bit	10x2 Diff +12 CMOS	Internal	170Mbit/s	85Mpix/s	~1440x900
		24bit	13x2 Diff +12 CMOS				
		30bit	16x2 Diff +12 CMOS				

(*1) Speed applies to panel interface only. (*2) Shared multi-standard IO cell is used.

(*3) These are only example resolutions. Maximum resolutions are determined by the maximum pixel frequencies.

Video Input Interfaces

Table 1.5. : SC1701BK3-200 Video Input Interfaces

#	Interface	Color depth	#Pins	Max Pin Freq.	Max Pix Freq.	Example resolution
1x	LVDS dual mode(*1)	18bit	8x2 Diff	560Mbit/s	160Mpix	~1920x1080
		24bit	10x2 Diff			
		30bit	12x2 Diff			
2x	LVDS single mode(*1)	18bit	4x2 Diff	1050Mbit/s	150Mpix	~1920x1080
		24bit	5x2 Diff			
		30bit	6x2 Diff			

(*1) Multi-standard IO cell is used

Capture pins are not shared with Display pins!

Table 1.6. : SC1701BH5-200 Video Input Interfaces

#	Interface	Color depth	#Pins	Max Pin Freq.	Max Pix Freq.	Example resolution
1x	LVDS dual mode(*1)	18bit	8x2 Diff	560Mbit/s	160Mpix	~1920x1080
		24bit	10x2 Diff			
		30bit(*2)	12x2 Diff			
1x	LVDS single mode(*1)	18bit	4x2 Diff	1050Mbit/s	150Mpix/s	~1920x1080
		24bit	5x2 Diff			
		30bit(*2)	6x2 Diff			

(*1)Multi-standard IO cell is used

(*2) Not supported by FPD0

Capture pins are not shared with Display pins!

Table 1.7. : SC1701BH5-300 Video Input Interfaces

#	Interface	Color depth	#Pins	Max Pin Freq.	Max Pix Freq.	Example resolution
1x	LVDS dual mode(*1)	18bit	8x2 Diff	490Mbit/s	140Mpix/s	~1920x1080
		24bit	10x2 Diff			
		30bit(*2)	12x2 Diff			
1x	LVDS single mode(*1)	18bit	4x2 Diff	980Mbit/s	140Mpix/s	~1920x1080
		24bit	5x2 Diff			
		30bit(*2)	6x2 Diff			

(*1)Multi-standard IO cell is used

(*2) Not supported by FPD0

Capture pins are not shared with Display pins!

1.3. Device Comparison

The following tables summarize the unique specifications of the SC1701BK3-200 and SC1701BH5-200/300.

1.3.1. General Features

Table 1.8. : General Feature Comparison

	SC1701BK3-200	SC1701BH5-200/300
FLASH memory	128kB	128kB
SRAM	256kB	256kB
Dimensions	23x23mm	24x24mm
Package	HS-BGA319	EP-LQFP216

1.3.2. Video-Related Features

Table 1.9. : Video-Related Features

	SC1701BK3-200	SC1701BH5-200	SC1701BH5-300
Number of display controllers	2	1	1
RSDS support	1x single/dual RSDS	1x single RSDS	1x single RSDS
LVDS support	2x single/dual LVDS	1x single/dual LVDS	1x single/dual LVDS
miniLVDS support	2x 3/6 pair miniLVDS	1x 3/6 pair miniLVDS	-
Max Htotal	16384	16384	16384
Max Vtotal	16384	16384	16384
Max Hactive	8192	4096	4096
Hactive per video pipeline	4096	4096	4096
Max Hactive (input for scaling)	2048	2048	2048
Max pixel clock	1x 533Mpix/s 2x 266Mpix/s	1x 160Mpix/s (*1)	1x 140Mpix/s
Example display resolution	1x 3840x2160 @ 60Hz 2x 2560x1600 @ 60Hz	1x 1920x1200 @ 60Hz	1x 1920x1080 @ 60Hz
Signature unit	up to 16 windows	up to 16 windows	up to 8 windows
Safety layer	Yes	Yes	Yes
Histogram unit	Yes	Yes	Yes
Color pipeline	10Bit / channel	10Bit / channel	10Bit / channel
(*1) Max pixel clock can be increased if customer ensures the appropriate thermal design.			

1.4. Block Diagrams

1.4.1. SC1701BK3-200 Overview Block Diagram

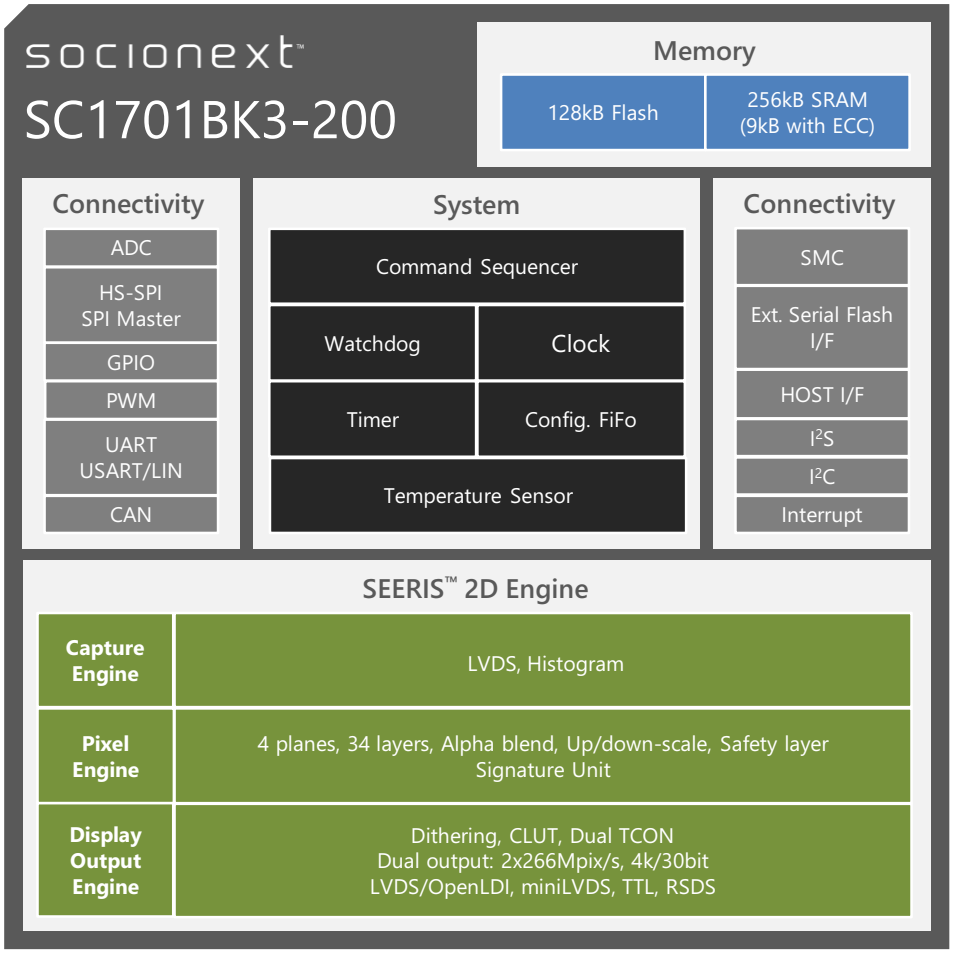

Figure 1.1. : SC1701BK3-200 block diagram

1.4.2. SC1701BH5-200 Overview Block Diagram

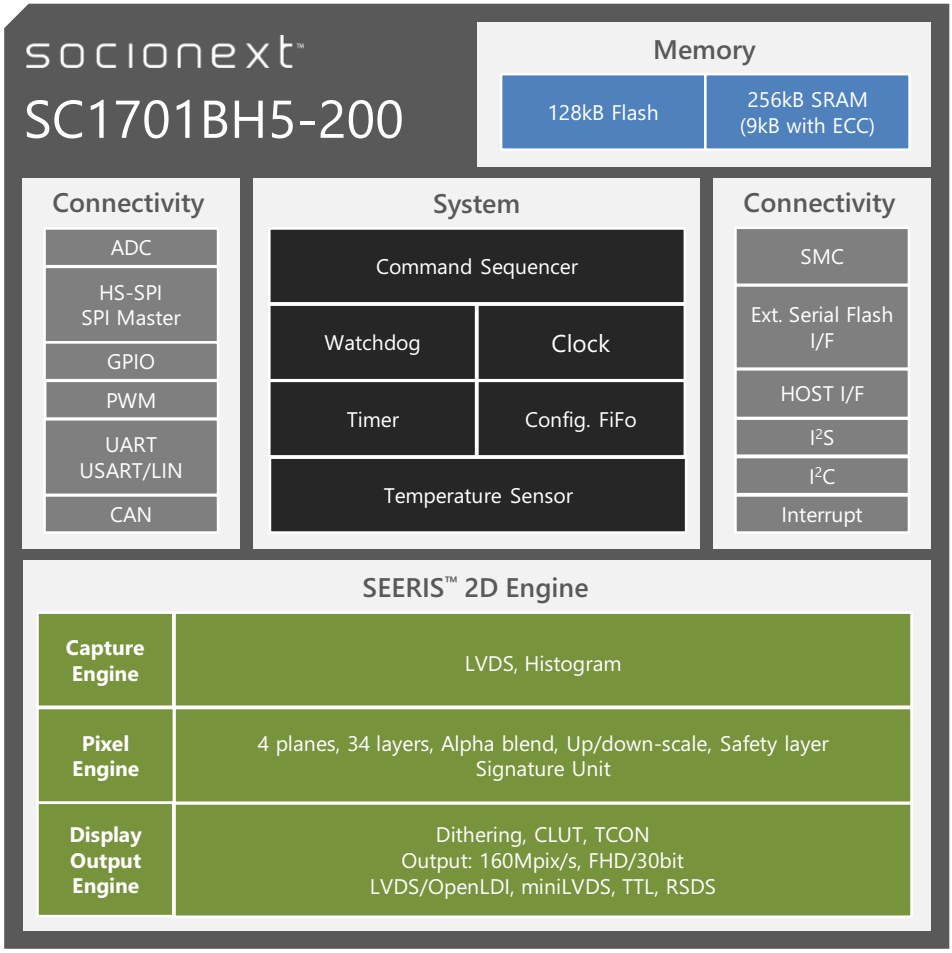

Figure 1.2. : SC1701BH5-200 block diagram

1.4.3. SC1701BH5-300 Overview Block Diagram

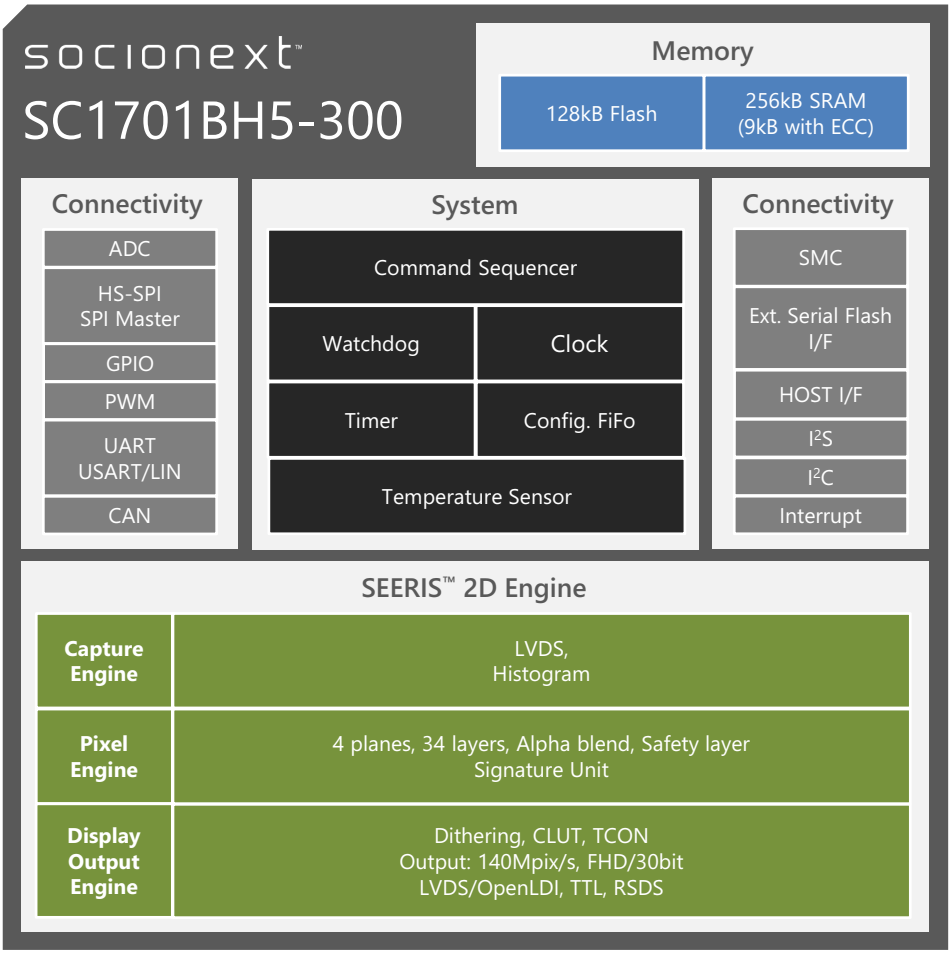

Figure 1.3. : SC1701BH5-300 block diagram

1.5. Package

1.5.1. SC1701BK3-200 Package

Table 1.10. : Package Characteristics

Package	HS-BGA
Pins	319
Dimensions	23 x 23 mm
Pitch	1 mm

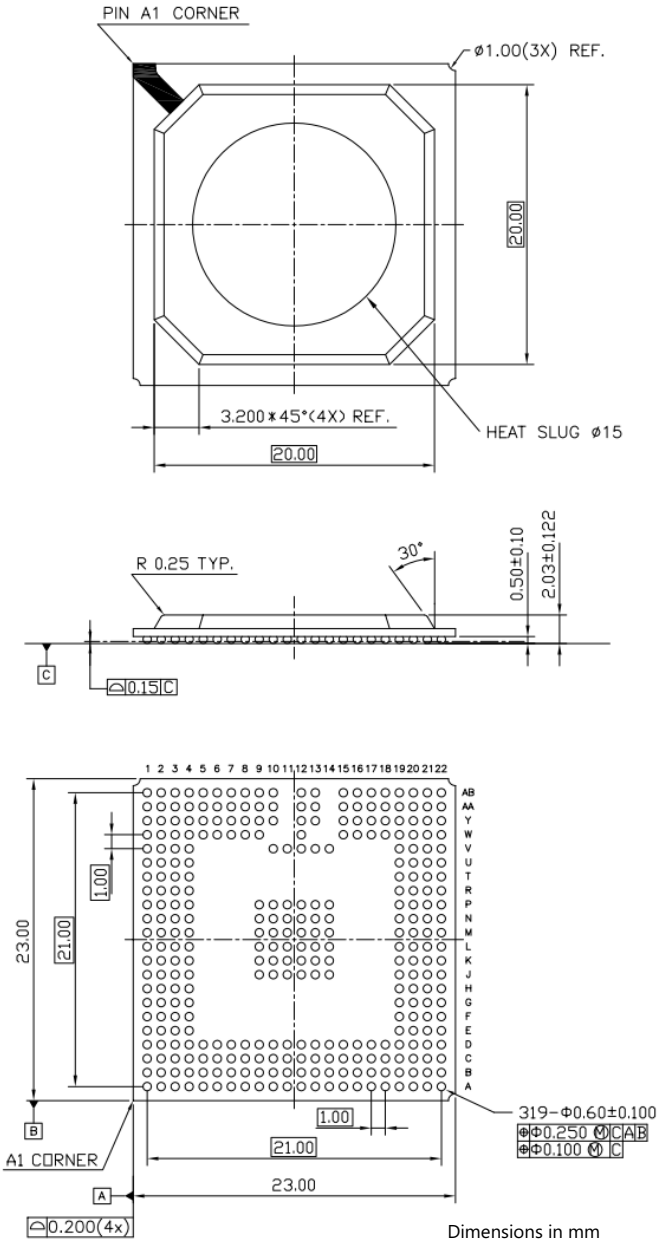

Figure 1.4. : SC1701BK3-200 Package

1.5.2. SC1701BH5-200/300 Package

Table 1.11. : Package Characteristics

Package	EP-LQFP
Pins	216
Dimensions	24x24 mm
Pitch	0.4 mm

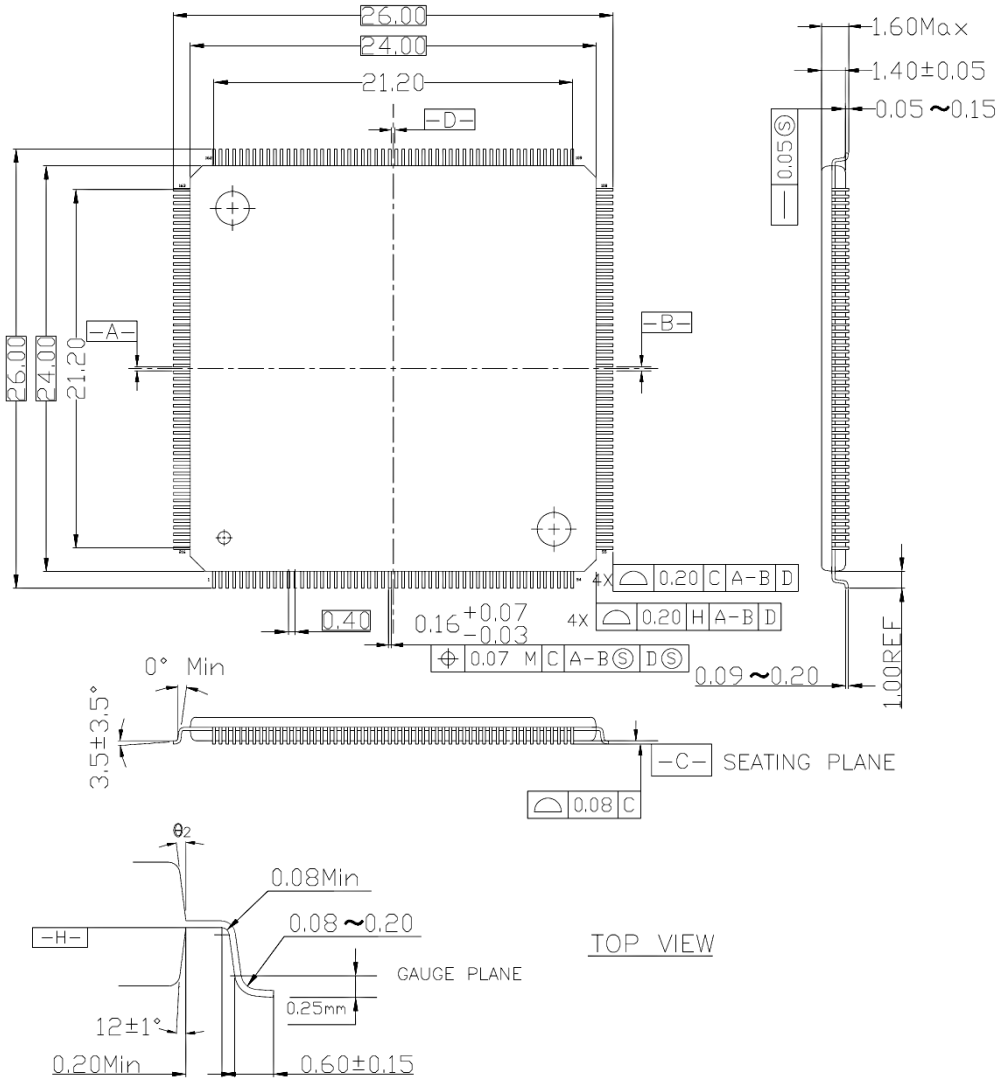

Figure 1.5. : SC1701BH5-200/300 Package (top view, dimensions in mm)

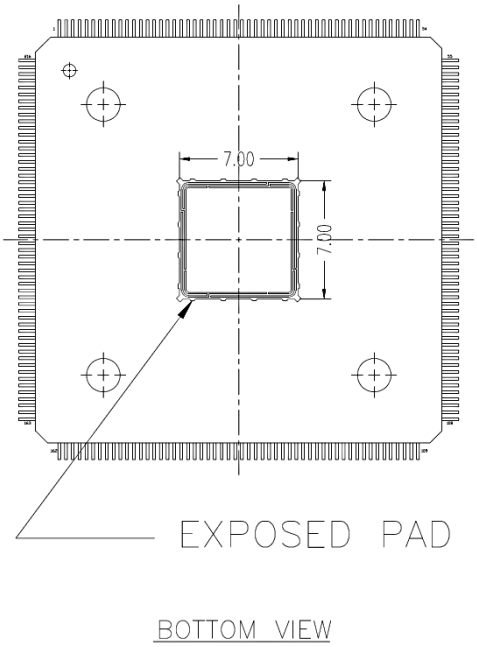

Figure 1.6. : SC1701BH5-200/300 Package (bottom view; dimensions in mm)

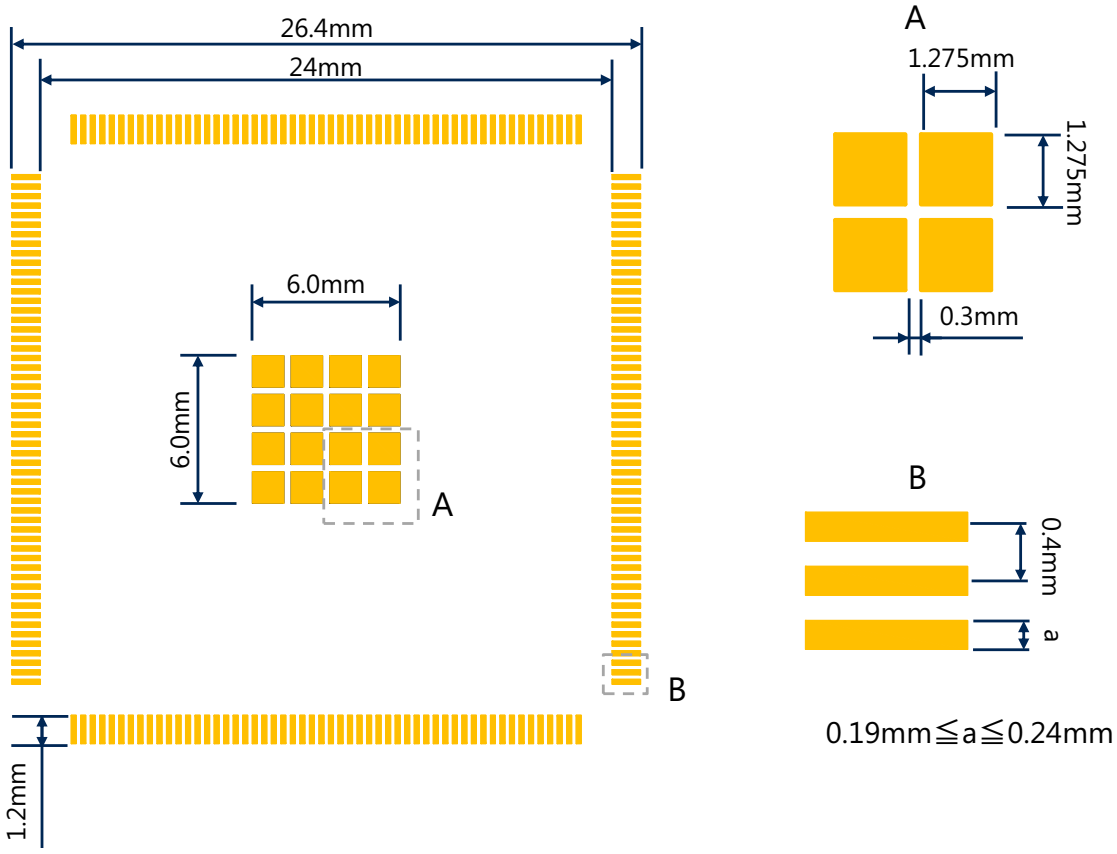

Figure 1.7. : SC1701BH5-200/300 - Exposed pad soldering pattern

1.6. Part Number Code

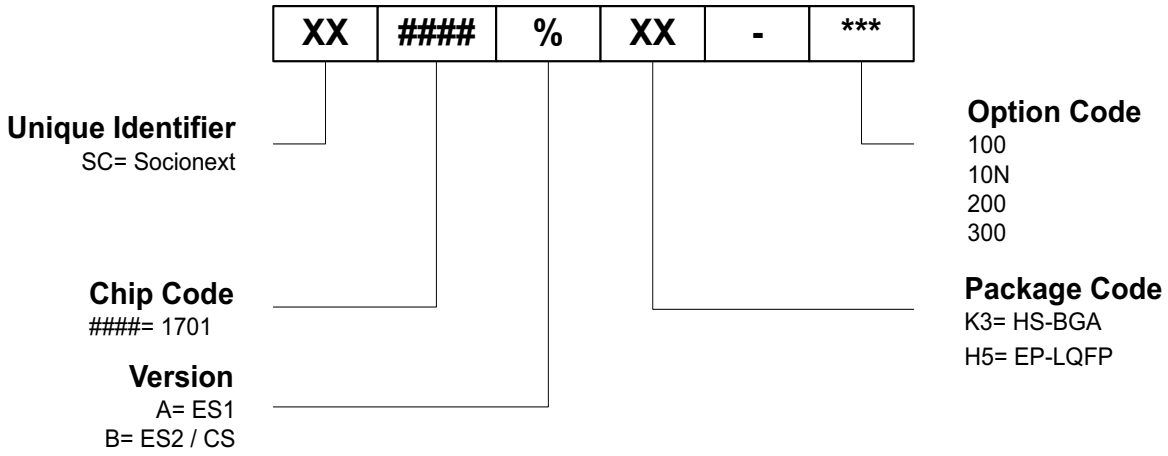

Figure 1.8. : Part number code

1.7. Pinning

1.7.1. SC1701BK3-200 Pin Overview

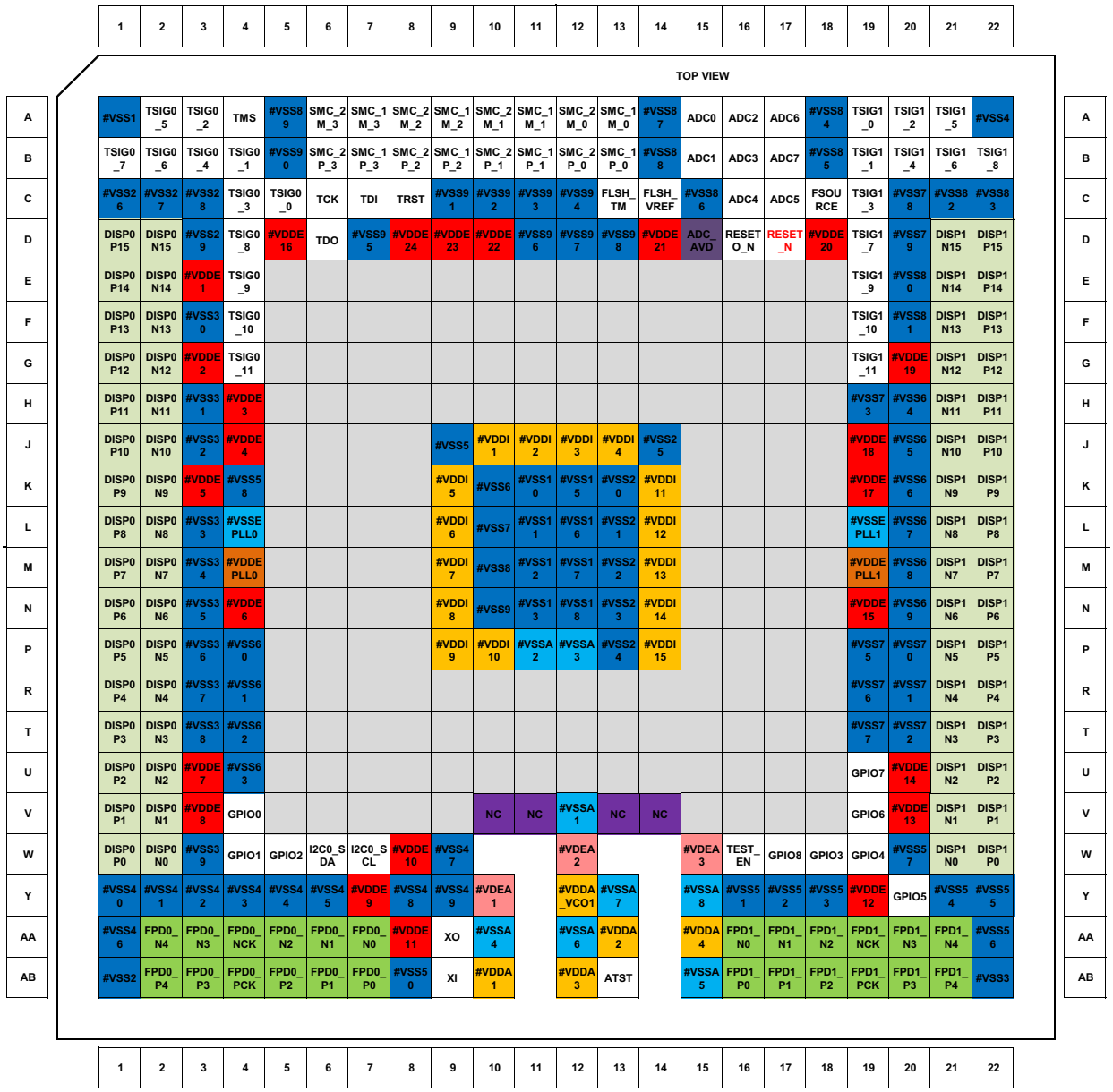

Figure 1.9. : SC1701BK3-200 Pin Overview

1.7.2. SC1701BH5-200/300 Pin Overview

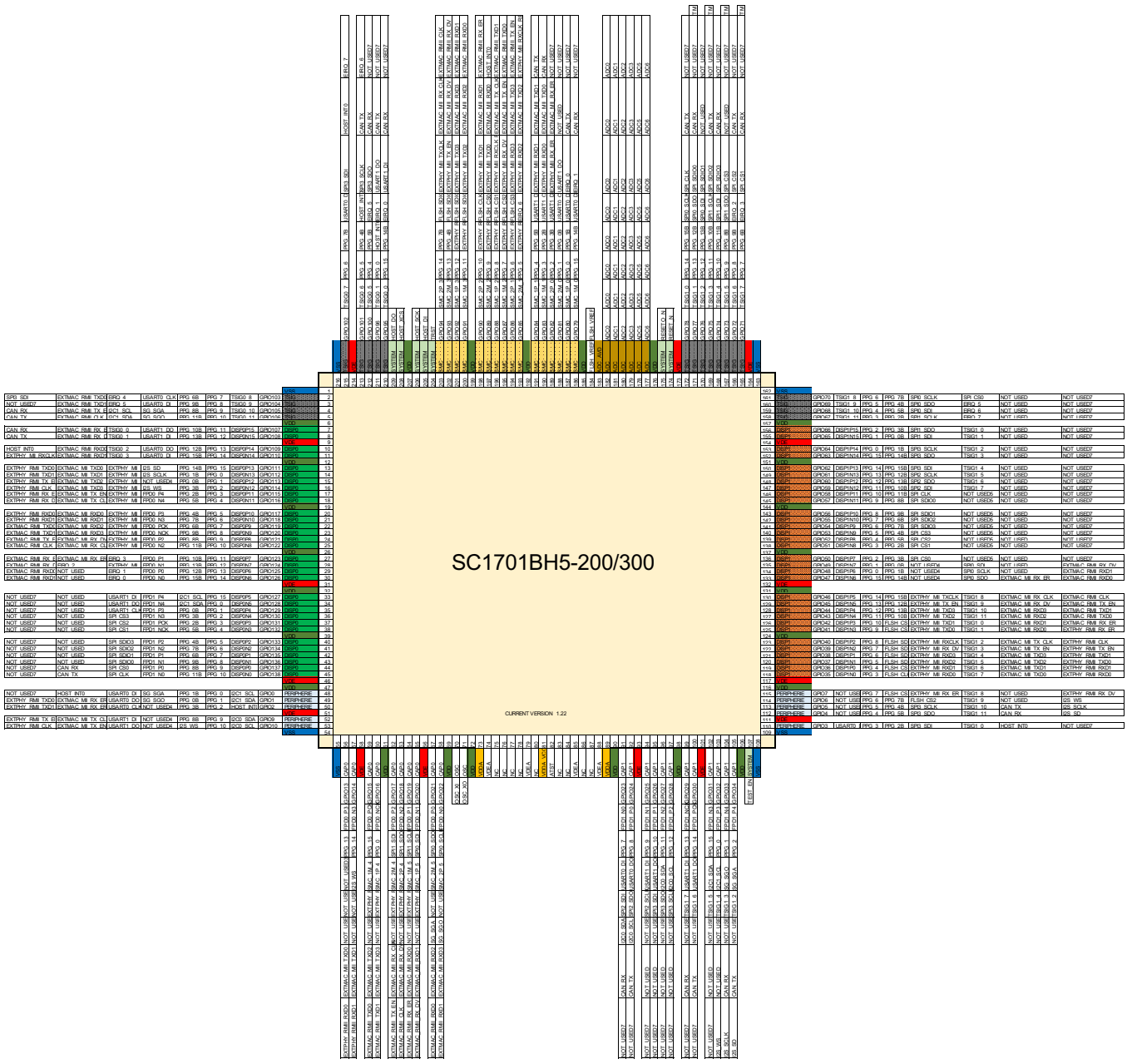

Figure 1.10. : SC1701BH5-200/300 Pin Overview (multiplex functionality). See attached file pinout_QFP216_X_v1.22.xlsx for a detailed view.

1.7.3. Pin Descriptions and Multiplexing

The functionality of many pins changes according to the pin multiplexing mode that is set.

SC1701BK3-200: For details refer to the attached pin table SC1701BK3-200_pinlist_v1.22.xlsx.

SC1701BH5-200: For details refer to the attached pin table SC1701BH5-200_pinlist_v1.22.xlsx.

SC1701BH5-300: For details refer to the attached pin table SC1701BH5-300_pinlist_v1.23.xlsx.

2. Electrical Characteristics

2.1. Operating Conditions

2.1.1. Absolute Maximum Ratings

Note: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of the absolute maximum ratings. Do not exceed these ratings.

Table 2.1. : Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Comment
Core supply	VDD	VSS -0.3	VSS+1.8	V	
IO supply	VDE	VSS -0.3	VSS+4.0	V	
VPLL DISP0 supply	VDDEPLL0	VSS -0.3	VSS+4.0	V	Only in SC1701BK3
VPLL DISP1 supply	VDDEPLL1	VSS -0.3	VSS+4.0	V	
ADC and bandgap reference supply	ADC_AVD	VSS -0.3	VSS+4.0	V	
PLL supply	VDEA	VSS -0.3	VSS+4.0	V	
PLL core supply	VDDA	VSS -0.3	VSS+1.8	V	
PLL VCO supply	VDDA_VCO	VSS -0.3	VSS+1.8	V	
Input voltage*	VI	VSS -0.3	VDE +0.3	V	
OSC input voltage	XI	VSS -0.3	VDD +0.3	V	
OSC output voltage	XO	VSS -0.3	VDD +0.3	V	
Analog input voltage	VIA	VSS -0.3	ADC_AVD + 0.3	V	< 4.0V
Output voltage	VO	VSS -0.3	VDE +0.3	V	< 4.0V
Storage temperature	T_{ST}	-55	150	°C	
Junction temperature	T_j	-40	150	°C	
* Input voltage of BID33-IO and MSIO (RSDS, LVDS, miniLVDS)					

Note:
- Applying stress exceeding the maximum ratings (voltage, current, temperature, etc.) may cause damage to semiconductor devices. Never exceed the ratings above.
- Never connect IC outputs or I/O pins directly, or connect them to VDD or VSS directly, otherwise thermal destruction of elements will result. This does not apply to pins designed to prevent signal collision.
- Provide ESD protection, such as grounding, when handling the product; otherwise externally charged electric charge flows inside the IC and discharges, which may result in damage to the circuit.
- Applying voltage higher than VDD or lower than VSS to I/O pins of CMOS IC, or applying voltage higher than the ratings between VDD and VSS may cause latch-up. The latch-up increases supply current, resulting in thermal destruction of elements. When handling the product, never exceed the maximum ratings.

2.1.2. Recommended Operating Conditions

Table 2.2. : Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Core supply	VDD	1.20	1.26	1.32	V	
IO supply	VDE	3.0	3.3	3.6	V	Including GPIOs, MSIOs, embedded flash
VPLL DISP0 supply	VDDEPLL0	3.0	3.3	3.6	V	Only in SC1701BK3
VPLL DISP1 supply	VDDEPLL1	3.0	3.3	3.6	V	
ADC and bandgap reference supply	ADC_AVD	3.0	3.3	3.6	V	Stable supply is needed for operation of embedded flash, POR and ADC
PLL supply	VDEA	3.0	3.3	3.6	V	
PLL core supply	VDDA	1.20	1.26	1.32	V	
PLL VCO supply	VDDA_VCO	1.20	1.26	1.32	V	
Ambient temperature	T_a	-40		105	°C	

2.2. Power Consumption

Table 2.3. : Power Consumption (estimated values)

Parameter	Symbol	Rating				Unit	Comment
		Min	Typ	Max SC1701BK3-200	Max SC1701BH5-200 SC1701BH5-300		
Core supply	I_{VDD}			1.80	1.20	A	
IO supply	I_{VDE}			0.70	0.46	A	BH5: DISP1, CAP1 VPLL, and CAP0 VPLL all active
VPLL0 supply	I_{VDDE_PLL0}			70	N/A	mA	BK3: Both DISP0 and CAP0 VPLL active
VPLL1 supply	I_{VDDE_PLL1}			70	N/A	mA	BK3: Both DISP1 and CAP1 VPLL active
ADC and bandgap reference supply	I_{ADC_AVD}			4	4	mA	
PLL analog supply	I_{VDDA}			185	185	mA	
PLL supply	I_{VDEA}			51	51	mA	
PLL VCO supply	I_{VDA_VCO}			7	7	mA	
N/A: Will not be available in SC1701BH5 chips.							

2.3. Thermal Design Considerations

Table 2.4 shows the estimated junction-to-ambient thermal resistance and junction-to-top-center-of-package thermal characterization. This thermal performance depends not only on the SC1701 package, but also on the characteristics of the PCB on which it is mounted.

Table 2.4. : Thermal Parameters

Device	Package	Θ_{JA}[°C/W]	Ψ_{JT}[°C/W]	Comment
SC1701BH5	EP-LQFP216	15.9	0.26	
SC1701BK3	TEBGA319	15.5	5.29	

PCB conditions: JEDEC PCB 4 layer 114.3x101.6x1.6mm, FloTHERM_JEDEC environment. The power consumption varies according to the application (i.e., depending on the use case).

2.4. Clock Input

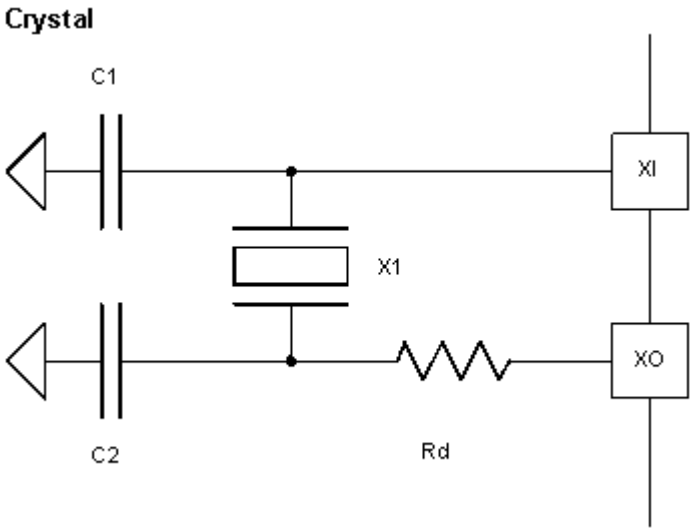

Figure 2.1. : Clock Input

Table 2.5. : Clock Input Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Crystal frequency	X1	-100 ppm	30	+100 ppm	MHz	(*2)
External load capacity	C1, C2		10		pF	Value depends on crystal
Damping resistor	Rd				Ohm	If needed, value depends on crystal
Input amplitude	V_{IH_XI}	0.8 * VDD			V	
	V_{IL_XI}			0.2 * VDD	V	
Figure of effort	EF			1.0		(*1)

(*1) $EF = f * C^{0.8} * R^{0.61}$ where

EF = figure of effort

f= frequency of oscillation

C= capacitive loading on XI and XO

R= crystal equivalent series resistance

Use the figure of effort equation (EF) to confirm that oscillation can be achieved at the target frequency for the specific loading characteristics (ESR, C) of the crystal in your design.

Note that the lower the calculated EF number is, the higher is the margin for the oscillator. The target EF number should be lower than the stated maximum to obtain more margin, recommended is EF < 0.8.

(*2) The listed accuracy is enough for the operation of typical video interfaces. If other interfaces, e.g. MII, need higher accuracy, then derive the necessary accuracy from the related blocks.

2.5. Reset Timing

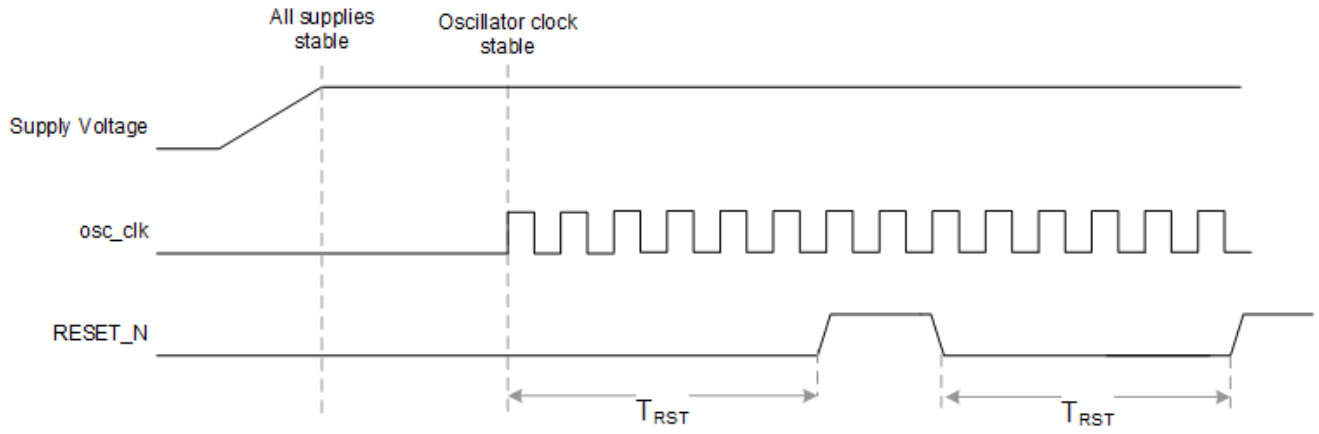

Figure 2.2. : Reset Timing

Table 2.6. : Timing Parameters Reset

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Reset low time	T_{RST}	1.0			ms	

2.6. Power-On Sequence

The figure below shows the power-On sequence and the groups of power supply that might be used, depending on the actual application.

VDD12 stands for the following supplies: VDD, VDDA, VDDA_VCO

VDDE stands for the following supplies: VDE, VDDE_PLL0, VDDE_PLL1, VDEA, ADC_AVD

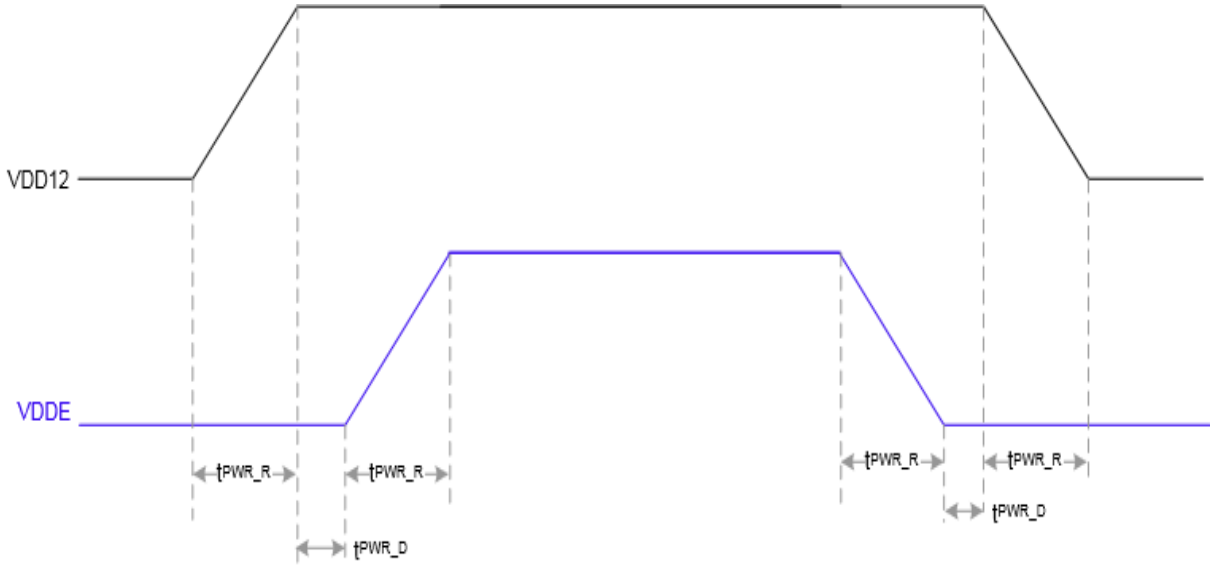

Figure 2.3. : Power-On Sequence

Table 2.7. : Power-On Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Power rise time	t_{PWR_R}	0.05		30	ms	
Power rise delay	t_{PWR_D}	0		1	s	
Power slew rate		0.1		20	mV/us	

2.7. Flash Memory Program / Erase Characteristics

Table 2.8. : Program/Erase time

Parameter	Value[1)]		Unit	Remarks
	Min	Max		
Sector erase time	16	20	ms	
Word programming time	16	20	µs	
[1)]Program/Erase cycle = Immediately after shipment				

Table 2.9. : Program/Erase cycle and data retention time[2)]

Program/Erase cycle at each sector		Data retention time	
Min value	Unit	Min value	Unit
1000	cycles	20	years
10000	cycles	10	years
[2)]These parameters are measured only for initial qualification.			

2.8. ADC Sampling Time

The SC1701 has an embedded 12-bit successive approximation ADC with an internal integrated sampling and holding stage. The signal will charge the sampling capacitor first and then the voltage signal on the sampling capacitor will be evaluated by the 12-bit ADC. The time to charge the sampling capacitor to its final value, equal to the signal level, is a function of the internal and external capacitor and resistor values. To reduce the error caused by the limited settling time to an acceptable level, the sampling time should be chosen much larger than the time constant to charge the sampling capacitor. The sampling time can be set with the ADC *TIMING.Tsample* register field.

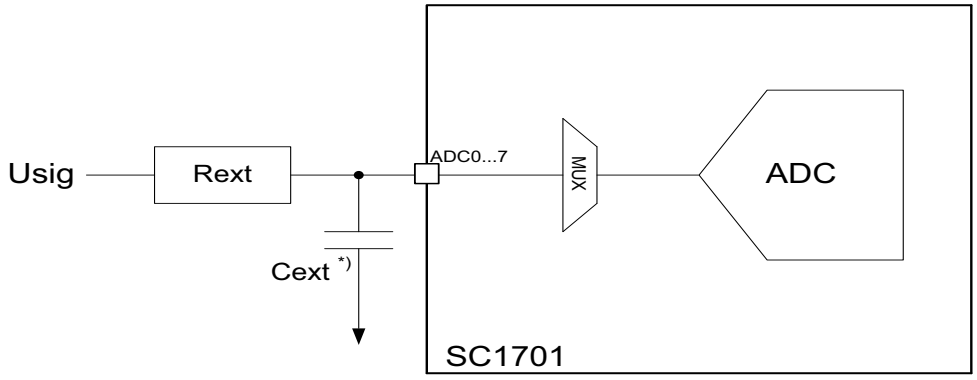

Figure 2.4. : ADC input signal

The minimum sampling time can be calculated with the following formula:

Example: When ADC_AVD = 3.3V (see Table 2.2 for ADC_AVD range).

For pins ADC0 ...ADC7 $Tsample[min] = F \times (46ns + (0.0135nF \times Rext\Omega) + (Rext\Omega \times CextnF))$

Table 2.10. : Factor F

ADC bit width	F
12 (default)	9.02
11	8.32
10	7.63
9	6.94
8	6.24
7	5.55
6	4.86
5	4.16
4	3.47
3	2.78
2	2.08
1	1.39

Note: The application requirements determine the ADC bit width and factor F can be derived from Table 2.10 .

With *Rext* = 0Ω

$$Tsample[min] = 415ns$$

Limitation

Tsample always < 10µs

2.8.1. ADC Electrical Characteristics

Table 2.11. : V_{AVDH} = 3.0V to 3.6V, Tj= -40°C to +150°C

Parameter	Symbol	Min	Typ	Max	Units
Performance					
Integral non-linearity	INL		±3.5	±4.5	LSB
Differential non-linearity	DNL		±2.5	±3.5	LSB
Zero transition error	V_{EZ}	-20		+20	mV
Full-scale transition error	V_{EF}	-20		+20	mV

2.8.2. Timing Characteristics

Table 2.12. : Timing characteristics

Parameter	Symbol	Min	Typ	Max	units
Sampling cycle	CYC_S	2			cycle
Sampling time	T_S	277		10000	ns
Conversion cycle	CYC_{CNV}		13		cycle
Wake-up time from power-down	T_{WU}	10			µs

The conversion rate is defined by the sum of the sampling cycle and the conversion cycle.

Example 1: When the sampling and conversion cycles are 5 and13 respectively, it means a 0.833 MS/s conversion rate at FCLK = 15 MHz.

Example 2: When the sampling and conversion cycles are 150 (max) and 13 respectively, it means a 0.092 MS/s conversion rate at FCLK = 15 MHz.

2.9. PCB Layout Recommendations

2.9.1. High Speed Interfaces

Please refer to the layout recommendations in Application Note “PCB Design Guideline”.

2.9.2. Configuration Pins

The following solutions are recommended when using the configuration pins.

Unused pin with pull-down

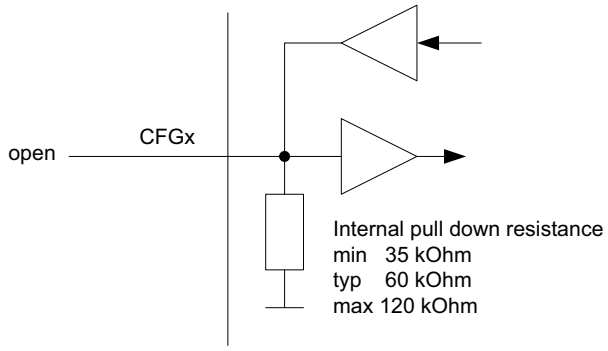

Figure 2.5. : Unused pin with pull-down

Unused pin with pull-up

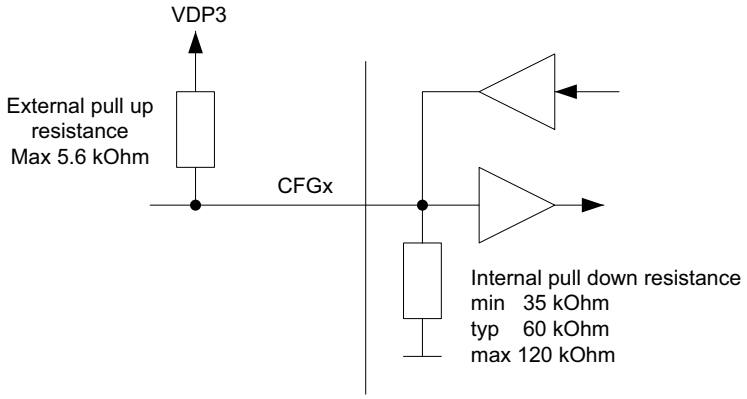

Figure 2.6. : Unused pin with pull-up

After power On, the internal pull-down must be switched Off to avoid power leakage.

Configuration pins are output - External device does not support pull-up

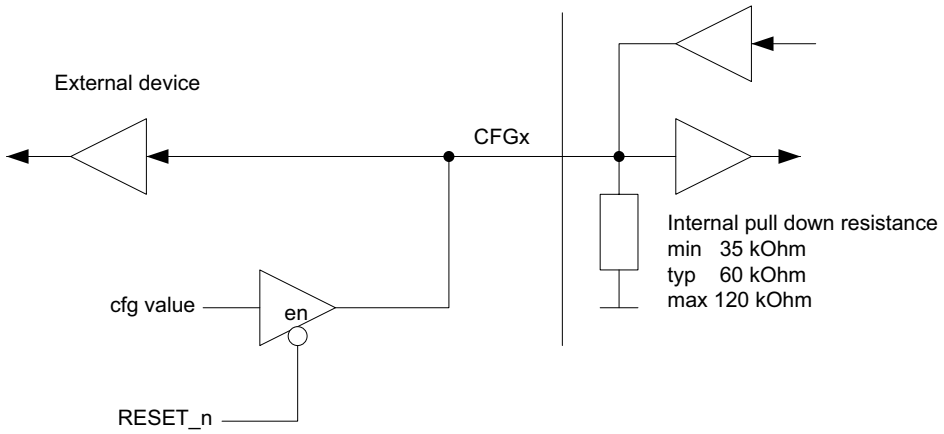

Figure 2.7. : Configuration pins are output

Note: The CFGx signal is latched 10us (260 osc_clk cycles after RESETN chip input released); therefore, disable CFG value driver 10us after chip reset release!

Configuration pins are input - External device does not support pull-up

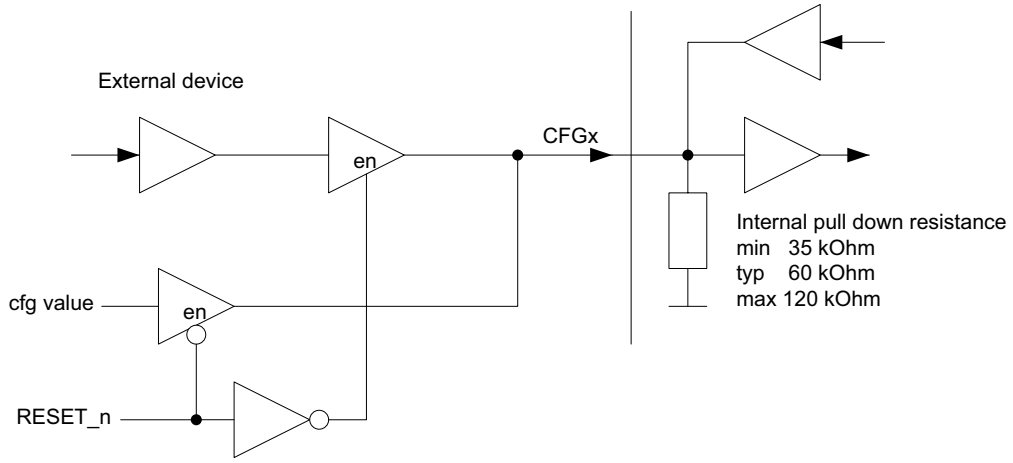

Figure 2.8. : Configuration pins are input

In this case, we recommend implementing a tri-state buffer on the board and an additional tri-state buffer in order to disconnect the external device from the CFG signals. After power On, the internal pull-down should be disconnected.

Note: The CFGx signal is latched 10us (260 osc_clk cycles after RESETN chip input released); therefore, disable CFG value driver 10us after chip reset release!

IO - External device does not support pull-up

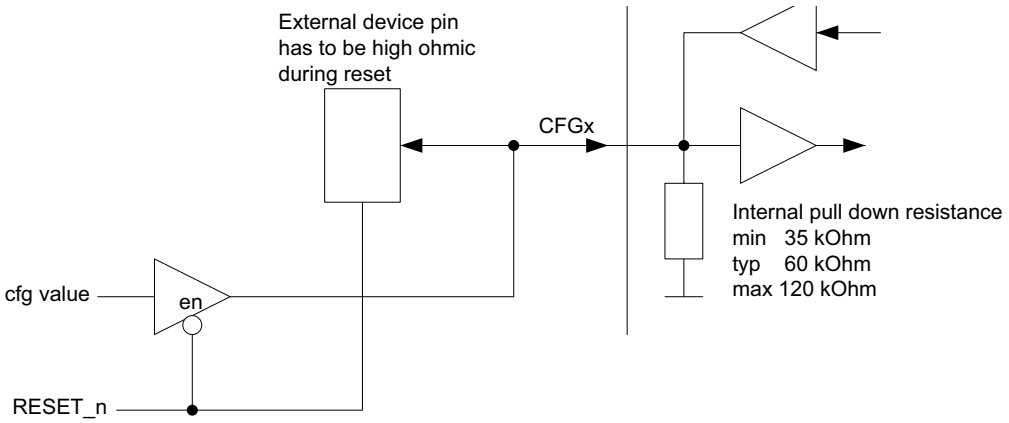

Figure 2.9. : IO - External device does not support pull-up

In this case, the external device must be in high-impedance state during reset. After power On, the internal pull-down should be disconnected.

Note: The CFGx signal is latched 10us (260 osc_clk cycles after RESETN chip input released); therefore, disable CFG value driver 10us after chip reset release!

2.10. AC Limits

2.10.1. Host SPI Characteristics

2.10.1.1. Host SPI Interface

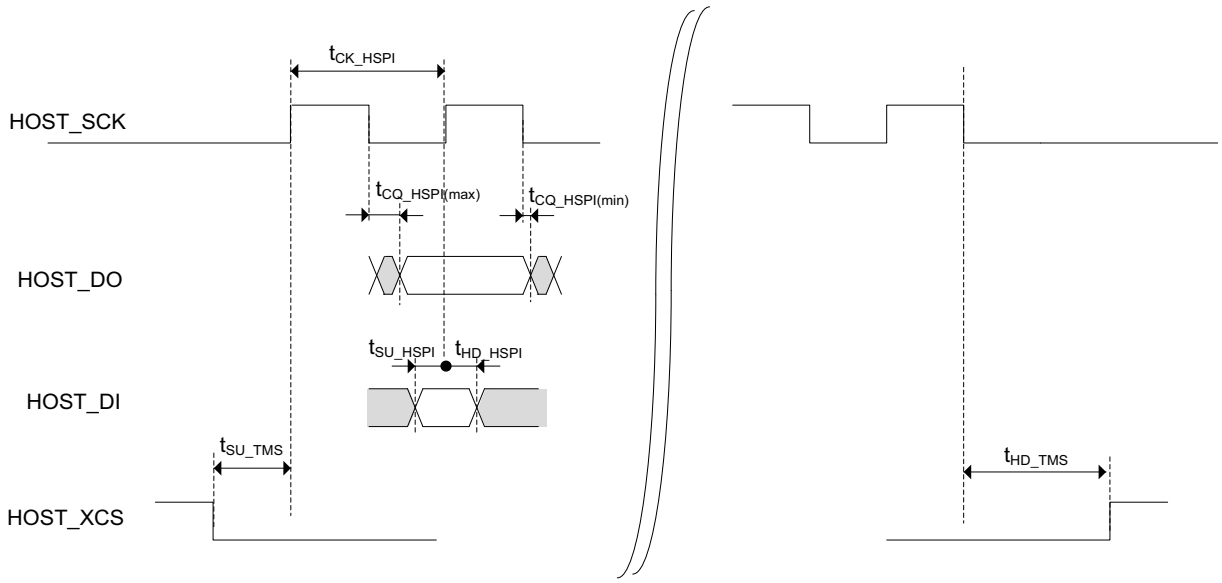

Figure 2.10. : Timing SPI interface

Table 2.13. : AC timing Host SPI interface

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
clk period	t_{CK_HSPI}	34			ns	Minimum 4 * HCLK period.
clk to output data	t_{CQ_HSPI}	0		20	ns	
Input data setup	t_{SU_HSPI}	10			ns	
Input data hold	t_{HD_HSPI}	5			ns	
Input Control setup	t_{HD_TMS}	50 + 2 * tHCLK			ns	
Input Control Hold	t_{HD_TMS}	50 + 2 * tHCLK			ns	

2.10.2. Config Interface

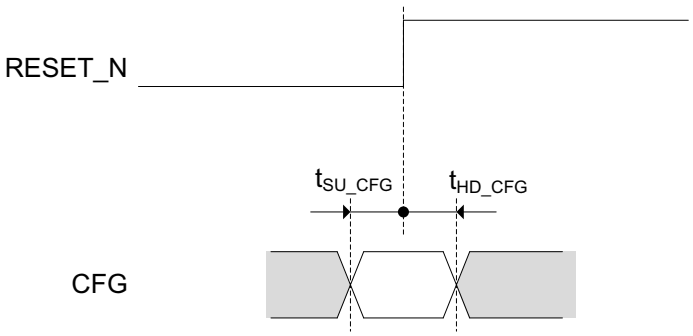

Figure 2.11. : Timing configuration pins

Table 2.14. : AC timing configuration pins

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
cfg data setup	t_{SU_CFG}	50			ns	
cfg data hold	t_{HD_CFG}	250			ns	

2.10.3. Display Interface

2.10.3.1. TTL Mode

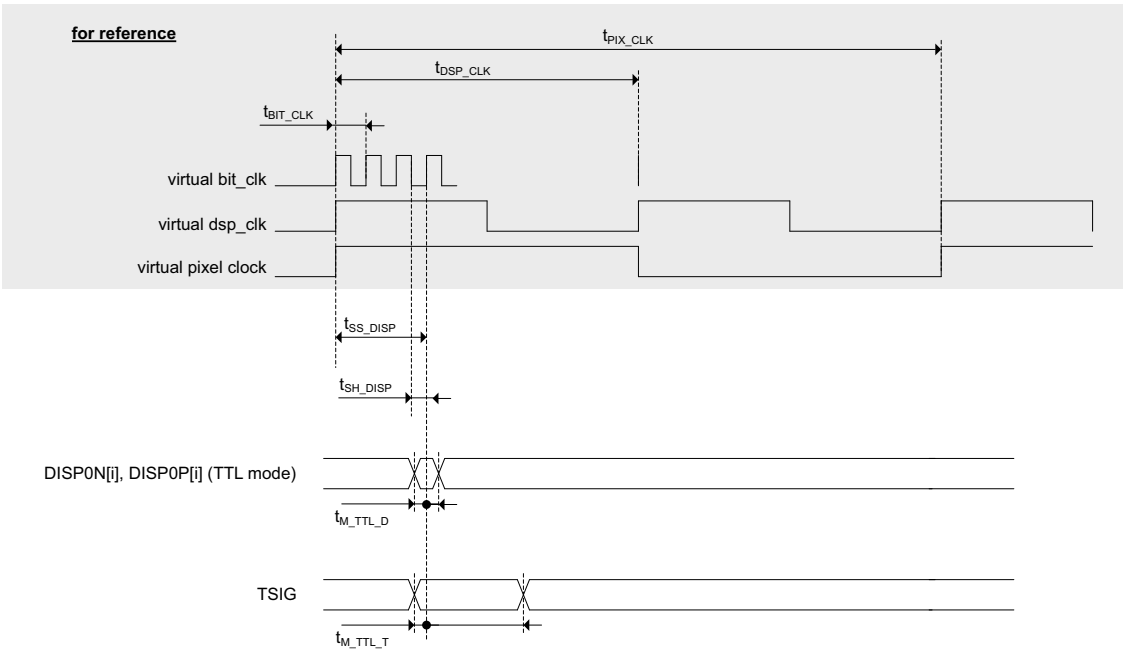

Figure 2.12. : Timing display TTL interface

Table 2.15. : AC timing TTL display interface

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
dsp_clk period	t_{DSP_CLK}	5.5			ns	Internal clock for reference only.
bit_clk period	t_{BIT_CLK}	1.8			ns	Internal clock for reference only, integer multiple of dsp_clk.
Pixel clock period	t_{PIX_CLK}	11	11.7		ns	Typical value is maximum pixel frequency, minimum value is due to spread spectrum and clock synthesis.
Shift value	t_{SS_DISP}	typ -150	$n \times t_{BIT\_CLK}$	typ + 150	ps	
Half cycle shift	t_{SH_DISP}	typ -200	$\frac{t_{BIT\_CLK}}{2}$	typ + 200	ps	
TTL DISP mismatch	$t_{M\_TTL\_D}$	-0.5		+0.5	ns	
TSIG TTL mismatch	$t_{M\_TTL\_T}$	1.5		4.5	ns	Related to center of DISP outputs.

2.10.3.2. RSDS Mode

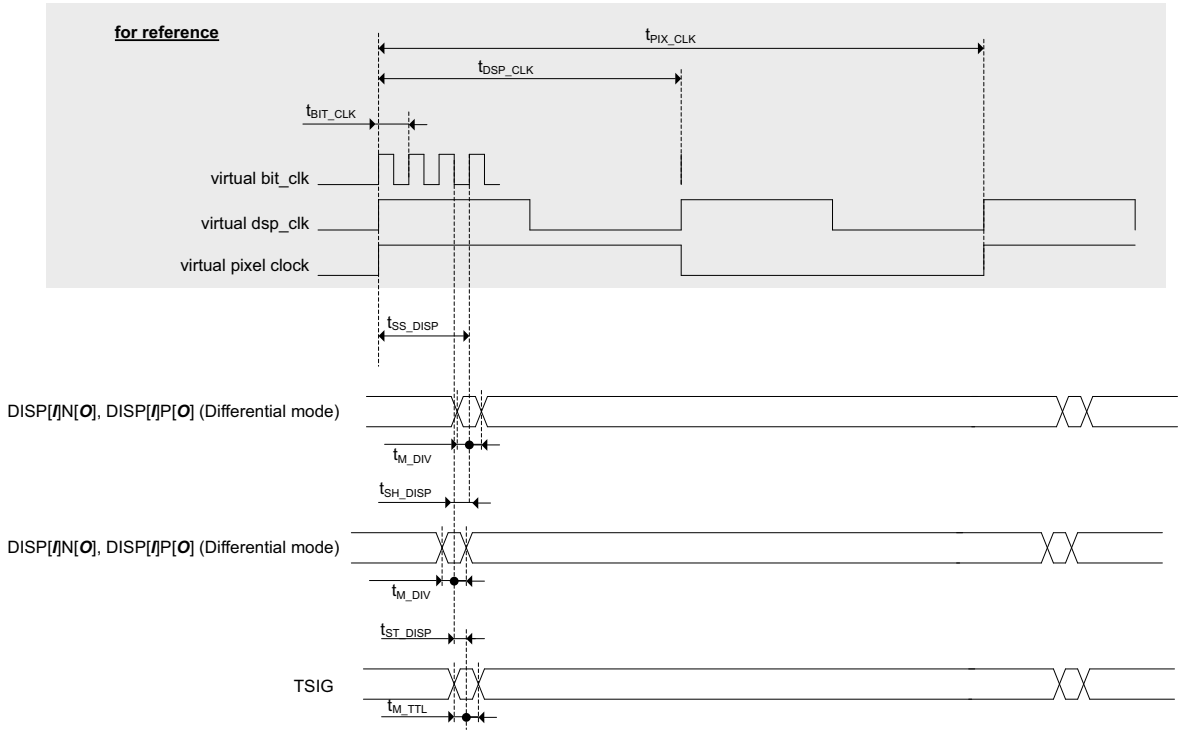

Figure 2.13. : Timing display RSDS interface

Table 2.16. : AC timings RSDS display interface

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
dsp_clk period	t_{DSP_CLK}	5.5			ns	Internal clock for reference only.
bit_clk period	t_{BIT_CLK}	1.8			ns	Internal clock for reference only, integer multiple of dsp_clk.
Pixel clock period	t_{PIX_CLK}	11	11.7		ns	Typical value is maximum pixel frequency, minimum value is due to spread spectrum and clock synthesis.
Shift value	t_{SS_DISP}	typ - 150	$n \times t_{BIT\_CLK}$	typ + 150	ps	
Half cycle shift	t_{SH_DISP}	typ - 200	$\frac{t_{BIT\_CLK}}{2}$	typ + 200	ps	
TSIG output mismatch	t_{M_TTL}	-1.0		+1.0	ns	
RSDS to TSIG shift	t_{ST_DISP}	0.4	2.5	4.6	ns	
RSDS output mismatch	t_{M_DIV}	-0.5		+0.5	ns	

2.10.3.3. LVDS Mode

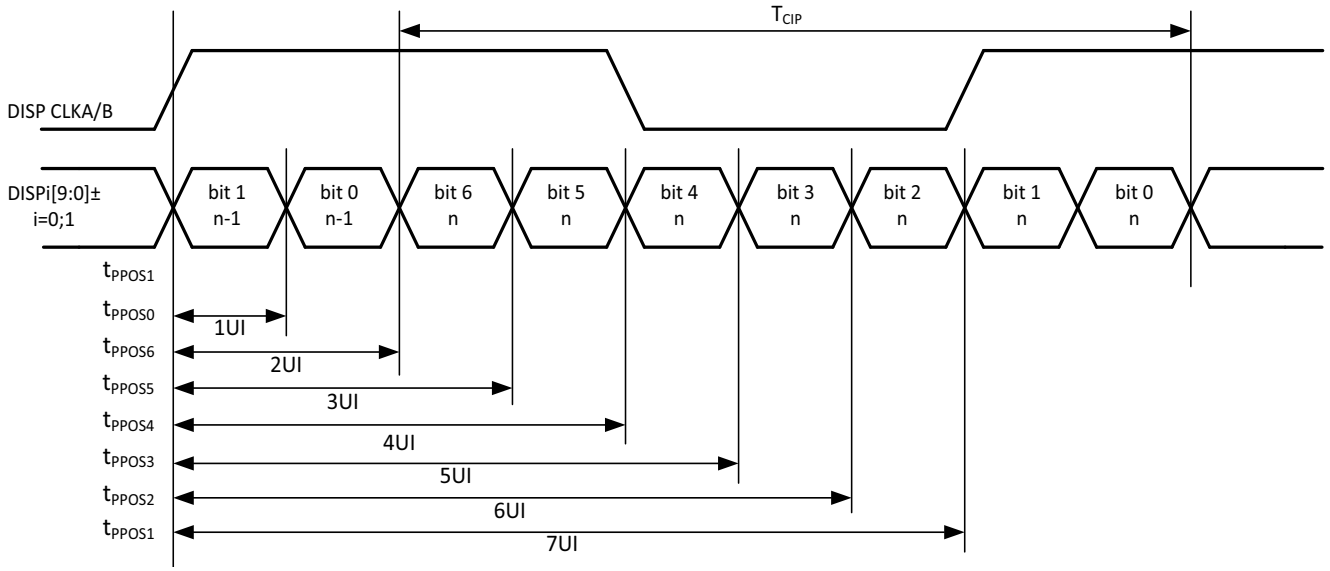

Figure 2.14. : FPD-link transmitter pulse positions

Table 2.17. : Transmitter switching characteristics

Symbol	Parameter	Min	Typ	Max	Units
TPPOS1	Transmitter Output Pulse for bit 1 (1st bit)	-0.15	0	+0.15	UI (*)
TPPOS0	Transmitter Output Pulse for bit 0 (2nd bit)	1 - 0.15	1	1 + 0.15	UI (*)
TPPOS6	Transmitter Output Pulse for bit 6 (3rd bit)	2 - 0.15	2	2 + 0.15	UI (*)
TPPOS5	Transmitter Output Pulse for bit 5 (4th bit)	3 - 0.15	3	3 + 0.15	UI (*)
TPPOS4	Transmitter Output Pulse for bit 4 (5th bit)	4 - 0.15	4	4 + 0.15	UI (*)
TPPOS3	Transmitter Output Pulse for bit 3 (6th bit)	5 - 0.15	5	5 + 0.15	UI (*)
TPPOS2	Transmitter Output Pulse for bit 2 (7th bit)	6 - 0.15	6	6 + 0.15	UI (*)
(*) A Unit Interval (UI) is defined as 1/7th of an ideal clock period (TCIP/7). The minimum TCIP is 7.50ns. Example: For a 7.50ns clock period (1.33.3MHz), 1 UI= 1.0714ns (see Figure 2.14).					

2.10.4. SPI Interface (External SPI and Flash SPI)

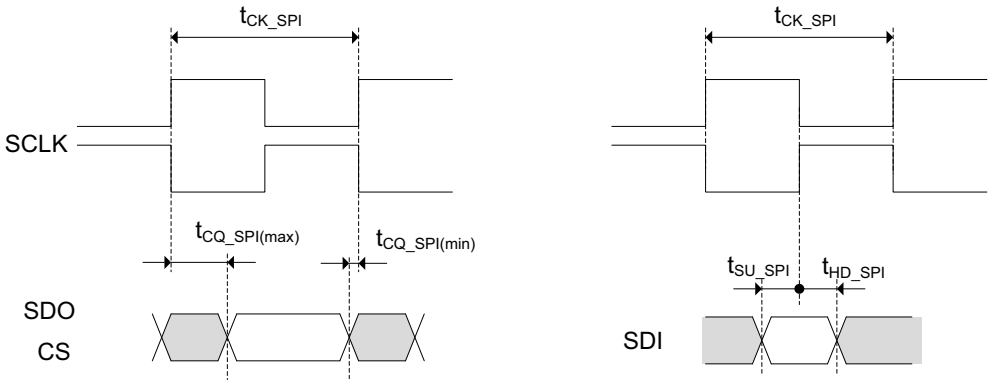

Figure 2.15. : Timing SPI interface

Table 2.18. : AC timings SPI interface

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
clk period	t_{CK_SPI}	25			ns	Period depends on selected AHB clock frequency.
clk to output data	t_{CQ_SPI}	-4		9.5	ns	Active clock edge depends on interface setup.
input data setup	t_{SU_SPI}	15 7.5			ns ns	Active clock edge depends on interface setup. No re-timing mode. Re-timing mode.
input data hold	t_{HD_SPI}	-3 2.5			ns ns	Active clock edge depends on interface setup. No re-timing mode. Re-timing mode.

2.10.5. I²C Interface

The SC1701BK3-200 / SC1701BH5-200/300 fulfills the timing requirements for the standard mode and fast mode of the Philips I²C specification.

The supply voltage to the I²C-bus lines (SDA and SCL) must not exceed the power-supply voltage of this I/O cell (VDE).

Voltage must not be supplied to the I²C-bus lines (SDA and SCL) if the power supply of this I/O cell (VDE) is Off.

2.10.6. USART/LIN Interface

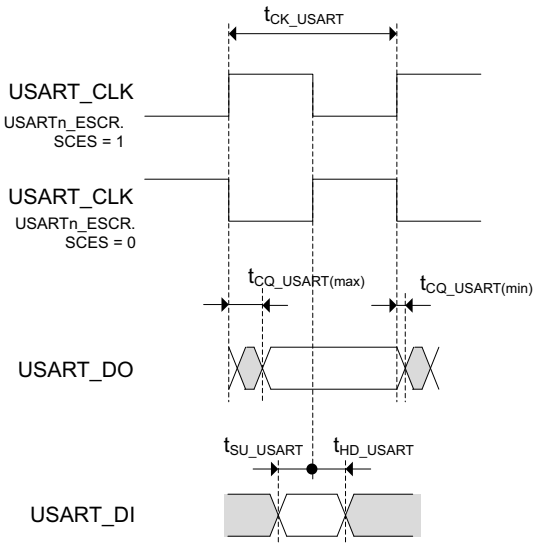

Figure 2.16. : Timing U(S)ART interface

Table 2.19. : AC timings U(S)ART interface

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
CLK period	t_{CK_USART}	4 x t_{rbus_clk}			ns	
CLK to output data	t_{CQ_USART}	-5		20 2 x t_{rbus_clk} + 45	ns	Internal CLK mode External CLK mode
Input data setup	t_{SU_USART}	t_{rbus_clk} + 25			ns	
Input data hold	t_{HD_USART}	t_{rbus_clk}			ns	

2.10.7. I²S Interface

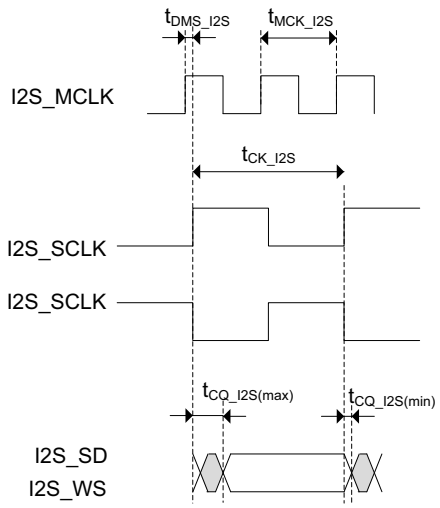

Figure 2.17. : Timing I²S interface

Table 2.20. : AC timings I²S interface

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
MCLK period	t_{MCK_I2S}	18.5			ns	
SCLK period	t_{CK_I2S}	37			ns	Half frequency of MCLK.
MCLK to SCLK delay	t_{DMS_I2S}	0		10	ns	
SCLK to output data	t_{CQ_I2S}	-5		10	ns	

2.10.8. MII Interface

All MIII AC timings are analyzed based on the pinmux groups M7-M11 EXTMAC_MII and M19-M22 EXTPHY_MII(see attachment Pinmux_MII_RMII.xlsx in Hardware Manual). For other pinmux settings the AC timing cannot be guaranteed.

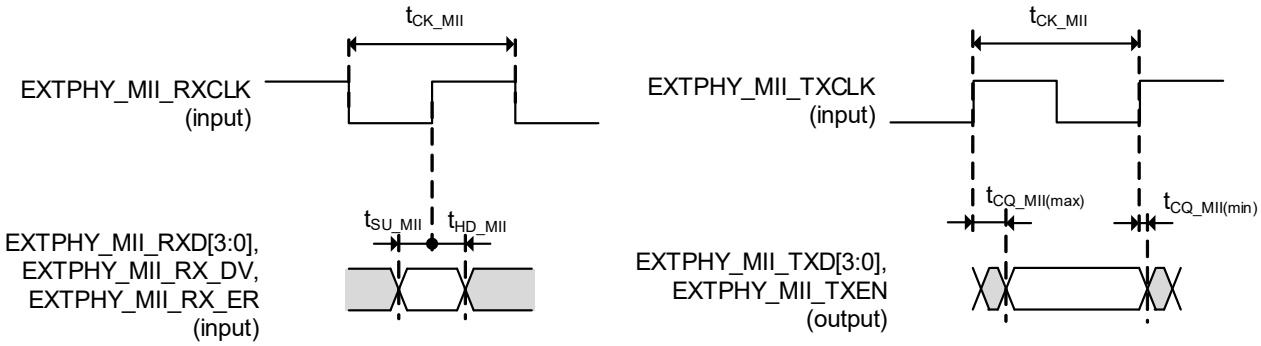

Figure 2.18. : AC Timing MII (external PHY)

Table 2.21. : AC Timing MII (external PHY)

Parameter	Symbol	Value			Unit	Comment
		Min	Typ	Max		
MII_CLK period	t_{CK_MII}		40 400		ns ns	100Mbit 10Mbit 2)
Output delay	t_{CQ_MII}	4		20	ns	1)
Input data setup	t_{SU_MII}	10			ns	2)
Input data hold	t_{HD_MII}	10			ns	2)
1) For 8mA drive strength setting, 20pF Load DISP* IOs, 30pF other IOs 2) Input transition 2.0ns						

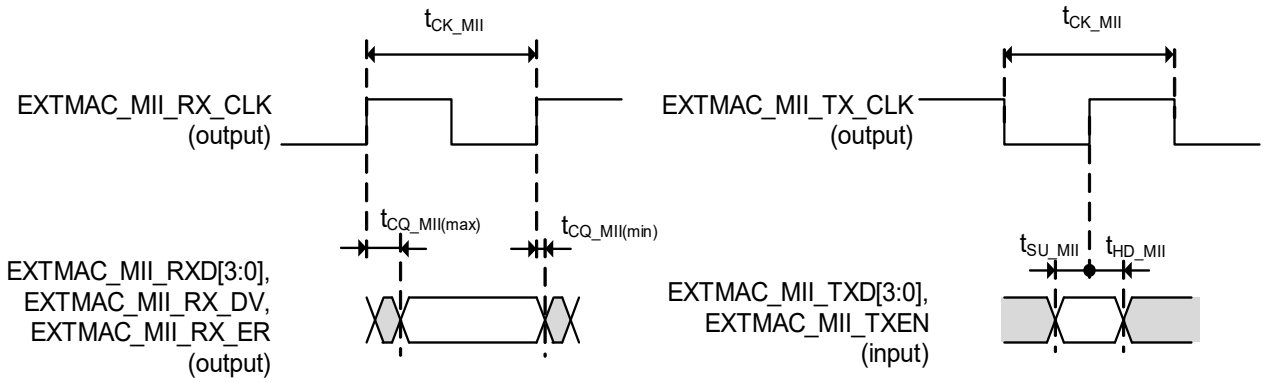

Figure 2.19. : AC Timing MII (internal PHY, external MAC is connected)

Table 2.22. : AC Timing MII (internal PHY)

Parameter	Symbol	Value			Unit	Comment
		Min	Typ	Max		
MII_CLK period (output)	t_{CK_MII}		40 400		ns ns	100Mbit 10Mbit 3)
Duty cycle		40%		60%		3)
Output delay	t_{CQ_MII}	12		23	ns	1)
Input data setup	t_{SU_MII}	10			ns	2)
Input data hold	t_{HD_MII}	0			ns	2)
1) For 8mA drive strength setting, 20pF Load DISP* IOs, 30pF other IOs 2) Input Transition 2.0ns , SMT=0 3) For maximum drive strength , 20pF Load DISP* IOs, 30pF other IOs						

2.10.9. RMII Interface

Only RMII reference clock output is supported.
All RMIII AC timings are analyzed based on the pinmux groups M1-M5 EXTMAC_RMII and M12-M16 EXTPHY _RMII(see attachment Pinmux_MII_RMII.xlsx in HM). For other pinmux settings the AC timing cannot be guaranteed.

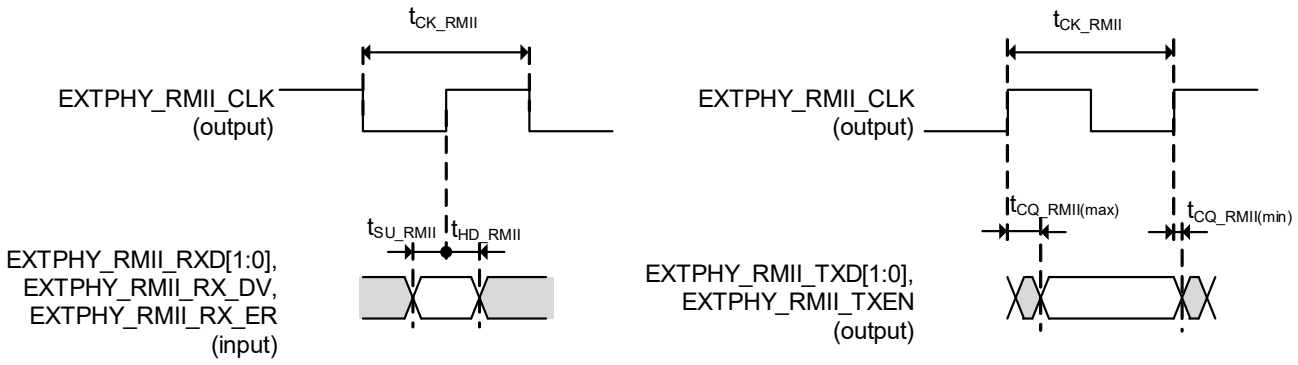

Figure 2.20. : AC Timing RMII (external PHY)

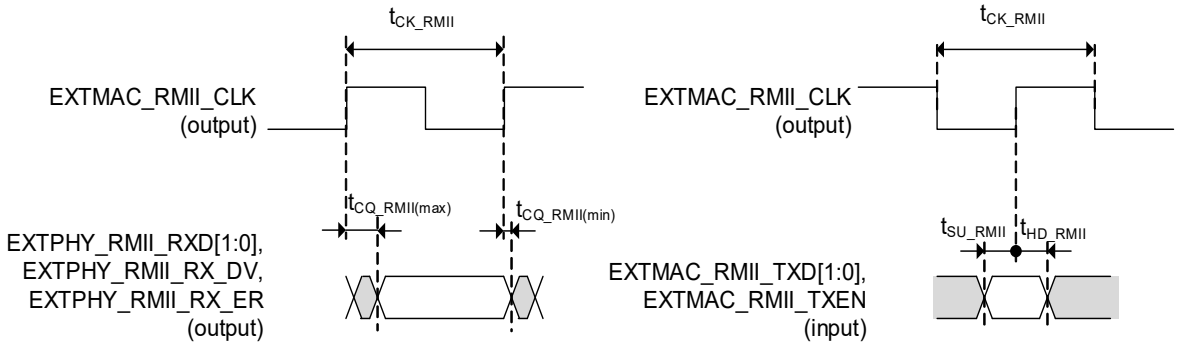

Figure 2.21. : AC Timing RMII (external MAC)

Table 2.23. : AC Timing RMII

Parameter	Symbol	Value			Unit	Comment
		Min	Typ	Max		
RMII CLK period	$t_{CK\ RMII}$		20		ns	100Mbit 2)
Duty cycle		35%		65%		2)
Output delay	$t_{CQ\ RMII}$	2		11	ns	1), 4)
Input data setup	$t_{SU\ RMII}$	4			ns	3)

Table 2.23. : AC Timing RMII (Continued)

Parameter	Symbol	Value			Unit	Comment
		Min	Typ	Max		
Input data hold	$t_{HD\ RMII}$	2			ns	3)
1) For 8mA drive strength setting, 20pF Load DISP* IOs, 30pF other IO 2) For maximum drive strength, 20pF Load DISP* IOs, 30pF other IO 3) Input Transition 2.0ns, SMT=0 4) Max output delay 13ns for M1 (TSIG0* DISP0* IOs)						

2.11. IO Circuit Types

This section goes over the different IO circuit types used in SC1701BK3-200 and SC1701BH5-200/300.

The different IO circuit types listed here correspond to the column “Pin Type” in the attached files SC1701BK3-200_pinlist_v1.22.xlsx, SC1701BH5-200_pinlist_v1.22.xlsx, and SC1701BH5-300_pinlist_v1.23.xlsx.

2.11.1. OSC

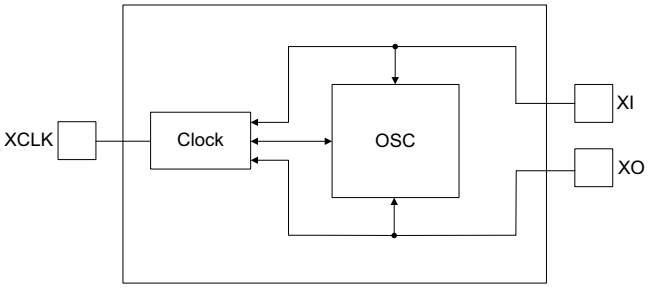

Figure 2.22. : Circuit type OSC

Characteristics:

- VDD supply domain
- High-speed oscillation circuit
- Input frequency: 30MHz APIX

2.11.2. INPUT, INPUTH

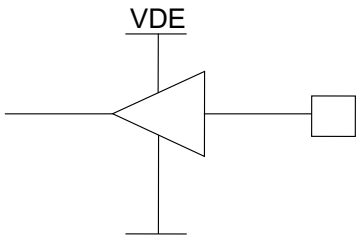

Figure 2.23. : Circuit type INPUT, INPUTH

Characteristics:

- VDE IO supply domain
- CMOS input

Parameter	Symbol	Min	Typ	Max
CMOS	VIH	0.8*VDE		VDE
	VIL	0V		0.2*VDE
Receiver hysteresis*	H	0.50V		0.65V
* parameter for INPUTH				

2.11.3. BIDI33

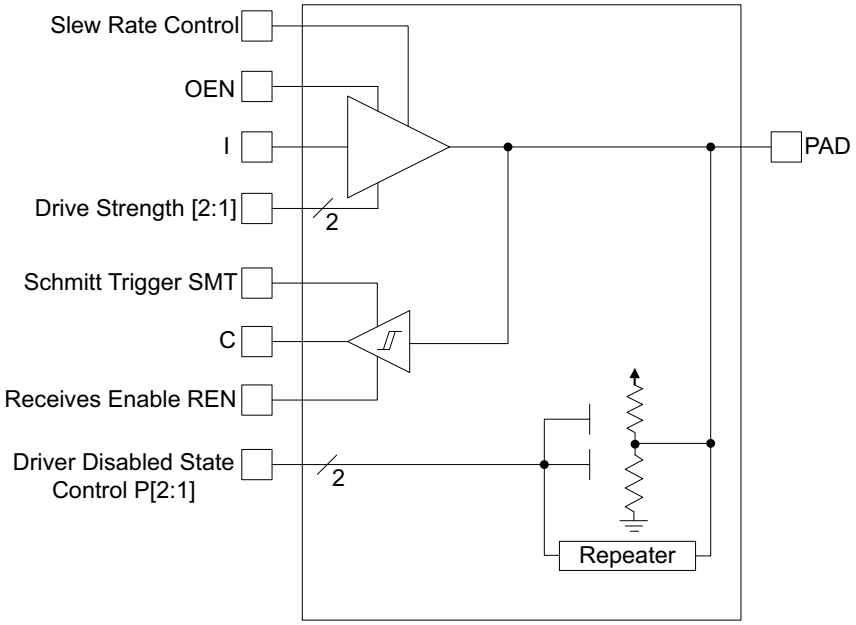

Figure 2.24. : Circuit type BIDI33

Characteristics:

- VDE IO supply domain
- CMOS level output

Parameter	Symbol	Min	Typ	Max
High output	VOH	VDE-0.5V		VDE
Low output	VOL	0V		0.4V

- Programmable output drive strength

Drive Setting	Symbol	Min	Typ	Max
00	IOL / IOH	2 ± 1mA		
01	IOL / IOH	4 ± 1mA		
10	IOL / IOH	8 ± 1mA		
11	IOL / IOH	12 ± 1mA		

- CMOS SCMITT input

Parameter	Symbol	Min	Typ	Max
CMOS	VIH	0.8*VDE		VDE
	VIL	0V		0.2*VDE

- Programmable pull-up and pull-down resistor

Parameter	Symbol	Min	Typ	Max
Pull-up / pull-down	R	35kOhm	60kOhm	120kOhm

2.11.4. Output

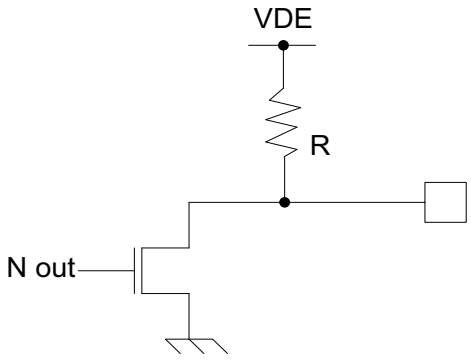

Figure 2.25. : Circuit type Output

Characteristics:

- VDE IO supply domain
- CMOS output level

Parameter	Symbol	Min	Typ	Max
High output	VOH	VDE-0.5V		VDE
Low output	VOL	0V		0.4V

- Output drive strength

Drive Setting	Symbol	Min	Typ	Max
	IOL	±1.5mA		
		Open drain *		
* for output drain output logic value “1”, Pull CMOS driver is switched to HIZ state				

- Pull-up resistor

Parameter	Symbol	Min	Typ	Max
Pull-up	R	20kOhm		50kOhm

2.11.5. Analog

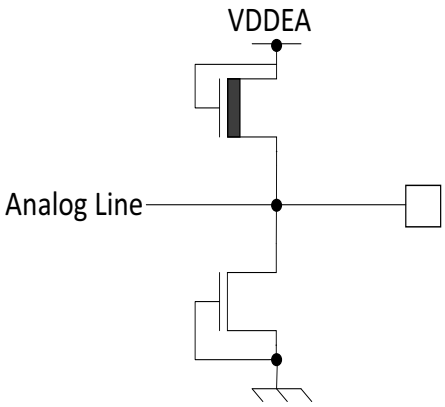

Figure 2.26. : Circuit type Analog

Characteristics:

- VDDEA IO supply domain
- Analog Pin
- Type INPUT: Analog input pin with ESD protection
- Type Output: Analog output line with ESD protection.

2.11.6. MSIO (Multi Standard IO)

2.11.6.1. LVDS TX

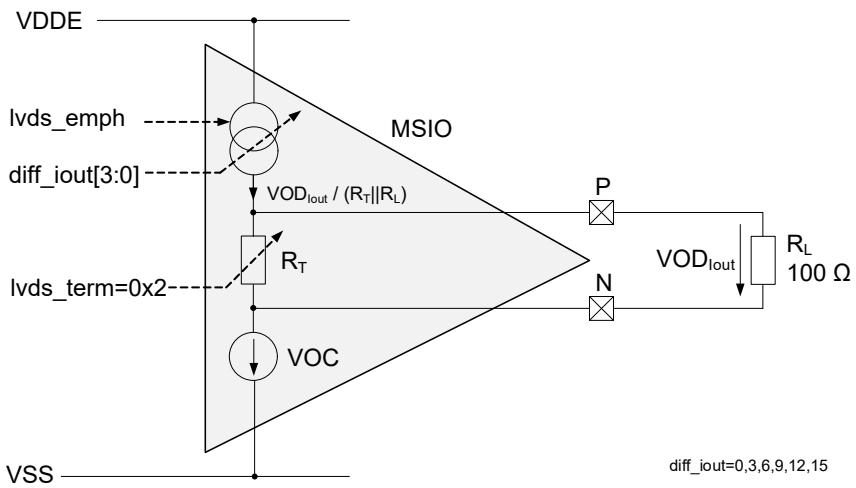

Figure 2.27. : Simplified circuit type MSIO LVDS TX

Table 2.24. : DC specifications for LVDS TX (over recommended operating conditions unless otherwise noted)

Parameter	Symbol	diff_iout[3:0]	lvds_emph	Condition	Limits		Unit
					Min	Max	
Differential Output Voltage	VOD0	0x0	0x0	Internal termination R_T enabled * External termination R_L=100Ω	85	182	mV
	VOD3	0x3	0x0		125	267	
	VOD6	0x6	0x0		164	353	
	VOD9	0x9	0x0		200	433	
	VOD12	0xC	0x0		229	514	
	VOD15	0xF	0x0		251	590	
	VOD0e	0x0	0x1		68	144	
	VOD3e	0x3	0x1		99	211	
	VOD6e	0x6	0x1		131	278	
	VOD9e	0x9	0x1		159	341	
	VOD12e	0xC	0x1		183	404	
	VOD15e	0xF	0x1		200	462	
Common Mode Voltage	VOC				1.00	1.50	V
Internal Termination	R_T				80	120	Ω
Registers relevant for LVDS TX ■ Setting for differential output voltage Iout: *DISP0.MSIOCTL_n.diff_iout_n* or *DISP1.MSIOCTL.n.diff_iout_n* (n=0...15). 16 registers are available; for each differential pair individual setup is possible. ■ * internal termination should be enabled by *DISP0.MSIOCTL.lvds_term* or *DISP1.MSIOCTL.lvds_term.* ■ For LVDS TX emphasis the relevant registers are *DISP0.MSIOCTL.lvds_emph* or *DISP1.MSIOCTL_emph*.							

The diagrams in Figure 2.28 show the emphasis impact on the LVDS signal wave form.

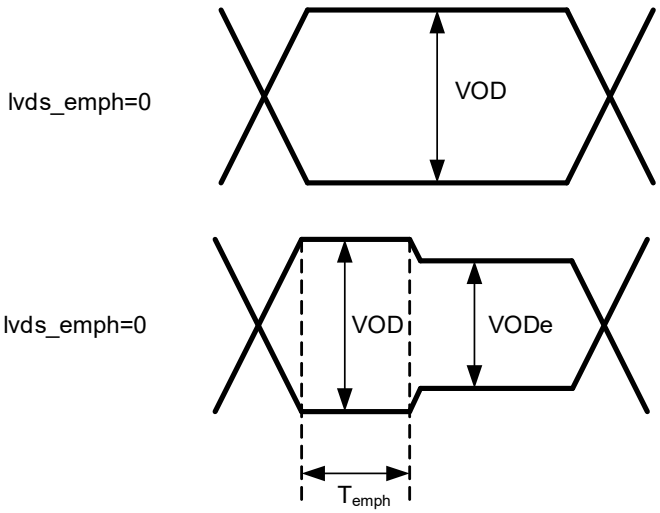

Figure 2.28. : LVDS signal wave form

The LVDS IO cell (MSIO) includes a driver that generates the nominal differential swing VOD. An additional delayed driver could drop swing level VOD to the level VODe in case the *lvds_emph* bit is set.

This function can improve the signal integrity, e.g., if longer cables are used.

Table 2.25. : AC Specifications (over recommended operating conditions unless otherwise noted)

Parameter	Symbol	Condition	Limits			Unit
			Min	Typ	Max	
LVDS Channel to Channel Skew	ChSkew				100	ps
Cycle to N-Cycle Jitter, N=7	Jcc				100	mUI
Pre-Emphasis Time	T_{emph}			1		ns

Note: For higher LVDS bandwidth (>600Mbps/lane) the EHS (Enable High Speed) should be enabled.

2.11.6.2. LVDS RX

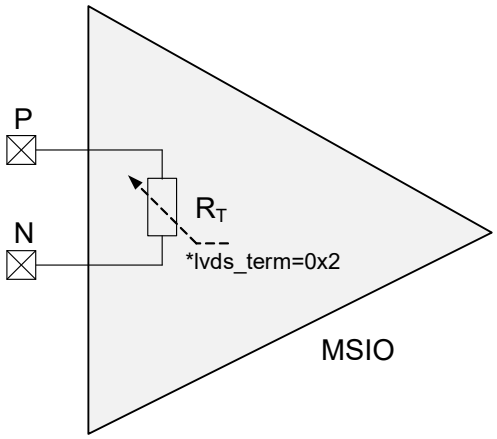

Figure 2.29. : Simplified circuit type MSIO LVDS RX

Table 2.26. : DC specifications (over recommended operating conditions unless otherwise noted)

Parameter	Symbol	Condition	Limits		Unit	Comment
			Min	Max		
Differential Input Swing	VOC	Internal termination R_T enabled	160	600	mV	VIH and VIL must not be violated
Input Common Mode	VIC		0.5	1.7	V	
Single-ended input high voltage	VIH			1.78	V	
Single-ended input low voltage	VIL		0.42		V	
Internal Termination	R_T		80	120	Ω	*lvds_term must be set to 0x02
Registers relevant for LVDS RX ■ For LVDS Iout the relevant registers are *CAP0.MSIOCTL_n.diff_iout_n* or *CAP1.MSIOCTL_n.diff_iout_n* (n=0...5). 6 registers are available; for each differential pair individual setup is possible. ■ The recommended value for LVDS capture is 0x9.						

2.11.6.3. miniLVDS TX

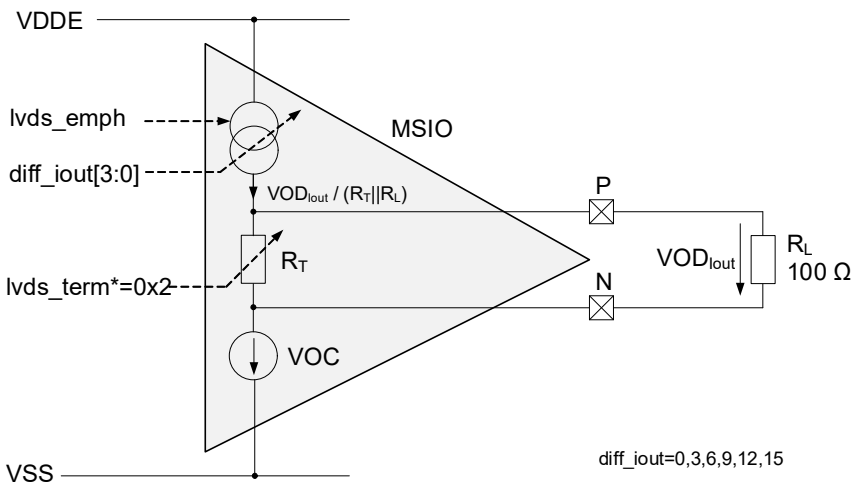

Figure 2.30. : Circuit type MSIO miniLVDS Tx

Table 2.27. : DC specifications for miniLVDS (over recommended operating conditions unless otherwise noted)

Parameter	Symbol	diff_iout[3:0]	lvds_emph	Condition	Limits		Unit
					Min	Max	
Differential Output Voltage	VOD9	0x9	0x0	Internal termination R_T enabled* External termination R_L=100Ω	200	433	mV
	VOD12	0xC	0x0		229	514	
	VOD15	0xF	0x0		251	590	
	VOD9e	0x9	0x1		159	341	
	VOD12e	0xC	0x1		183	404	
	VOD15e	0xF	0x1		200	462	
Common Mode Voltage	VOC				1.00	1.50	V
Internal Termination	R_T				80	120	Ω

Registers relevant for LVDS TX

- Setting for differential output voltage Iout: *DISP0.MSIOCTL_n.diff_iout_n* or *DISP1.MSIOCTL.n.diff_iout_n* (n=0...15). 16 registers are available, for each differential pair individual setup is possible.
- * internal termination should be enabled by *DISP0.MSIOCTL.lvds_term* or *DISP1.MSIOCTL.lvds_term.*
- For LVDS TX emphasis the relevant registers are *DISP0.MSIOCTL.lvds_emph* or *DISP1.MSIOCTL.lvds_emph*.

The diagrams in Figure 2.31 show the emphasis impact on the LVDS signal wave form.

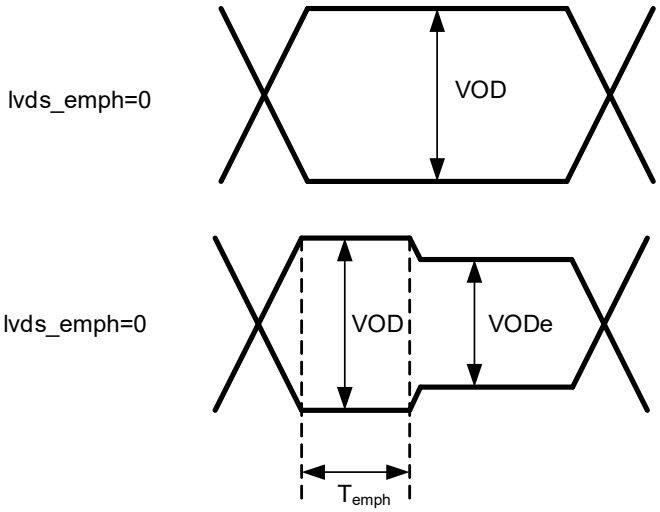

Figure 2.31. : LVDS signal wave form

The LVDS IO cell (MSIO) includes a driver that generates the nominal differential swing VOD. An additional delayed driver could drop swing level VOD to the level VODe in case the *lvds_emph* bit is set.

This function can improve the signal integrity, e.g., if longer cables are used.

Table 2.28. : AC Specifications (over recommended operating conditions unless otherwise noted)

Parameter	Symbol	Condition	Limits			Unit
			Min	Typ	Max	
LVDS Channel to Channel Skew	ChSkew				100	ps
Cycle to N-Cycle Jitter, N=7	Jcc				100	mUI
Pre-Emphasis Time	T_{emph}			1		ns

Note: For higher LVDS bandwidth (>600Mbps/lane) the EHS (Enable High Speed) should be enabled.

2.11.6.4. RSDS TX SST (Single Sided Termination)

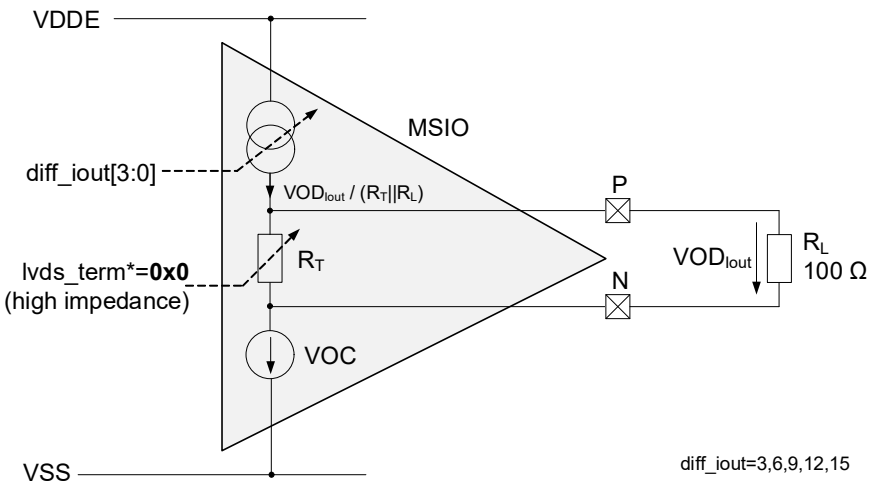

Figure 2.32. : Circuit type MSIO RSDS TX SST

Table 2.29. : DC specifications (over recommended operating conditions unless otherwise noted)

Parameter	Symbol	diff_iout[3:0]	lvds_emph	Condition	Limits		Unit
					Min	Max	
Differential Output Voltage	VOD0	0x0	0x0	Internal termination R_T disabled (high impedance) * External termination R_L=100Ω	167	330	mV
	VOD3	0x3	0x0		245	485	
Common Mode Voltage	VOC				1.00	1.50	V
Internal Termination	R_T				high impedance		Ω

Relevant registers for RSDS TX (SST)

- Setting for differential output voltage Iout: *DISP0.MSIOCTL_n.diff_iout_n* or *DISP1.MSIOCTL_n.diff_iout_n* (n=0...15). 16 registers are available; for each differential pair individual setup is possible.
- * the internal termination should be enabled by *DISP0.MSIOCTL.lvds_term* or *DISP1.MSIOCTL.lvds_term*.
- For LVDS TX emphasis the relevant registers are *DISP0.MSIOCTL.lvds_emph* or *DISP1.MSIOCTL.lvds_emph*.

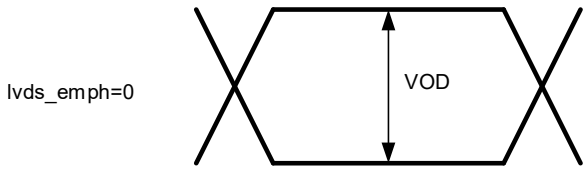

Figure 2.33. : RSDS signal wave form

Table 2.30. : AC Specifications (over recommended operating conditions unless otherwise noted)

Parameter	Symbol	Condition	Limits			Unit
			Min	Typ	Max	
LVDS Channel to Channel Skew	ChSkew				100	ps
Cycle to N-Cycle Jitter, N=7	Jcc				100	mUI

2.11.6.5. RSDS TX DST (Double Sided Termination)

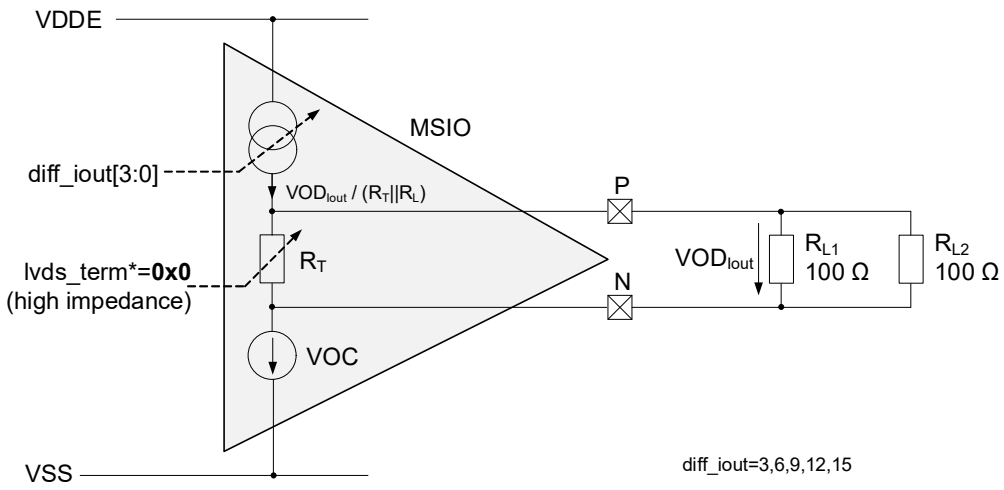

Figure 2.34. : Circuit type MSIO RSDS TX DST

Table 2.31. : DC specifications (over recommended operating conditions unless otherwise noted)

Parameter	Symbol	diff_iout[3:0]	lvds_emph	Condition	Limits		Unit
					Min	Max	
Differential Output Voltage	VOD3	0x3	0x0	Internal termination R_T disabled (high impedance) * External termination RL1 || RL2 = 100Ω ||100Ω	125	267	mV
	VOD6	0x6	0x0		164	353	
	VOD9	0x9	0x0		200	433	
	VOD12	0xC	0x0		229	514	
	VOD15	0xF	0x0		251	590	
Common Mode Voltage	VOC				1.00	1.50	V
Internal Termination *	R_T				high impedance		Ω

Relevant registers for RSDS TX (DST):

- Setting for differential output voltage Iout: *DISP0.MSIOCTL_n.diff_iout_n* or *DISP1.MSIOCTL_n.diff_iout_n* (n=0...15). 16 registers are available; for each differential pair individual setup is possible.
- * the internal termination should be enabled by registers: *DISP0.MSIOCTL.lvds_term* or *DISP1.MSIOCTL.lvds_term*.

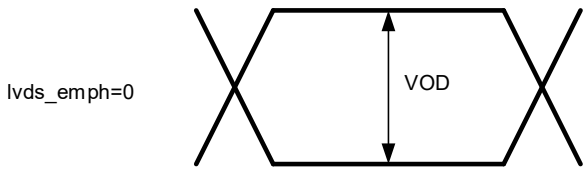

Figure 2.35. : RSDS signal wave form

Table 2.32. : AC Specifications (over recommended operating conditions unless otherwise noted)

Parameter	Symbol	Condition	Limits			Unit
			Min	Typ	Max	
LVDS Channel to Channel Skew	ChSkew				100	ps
Cycle to N-Cycle Jitter, N=7	Jcc				100	mUI

2.11.6.6. TTL

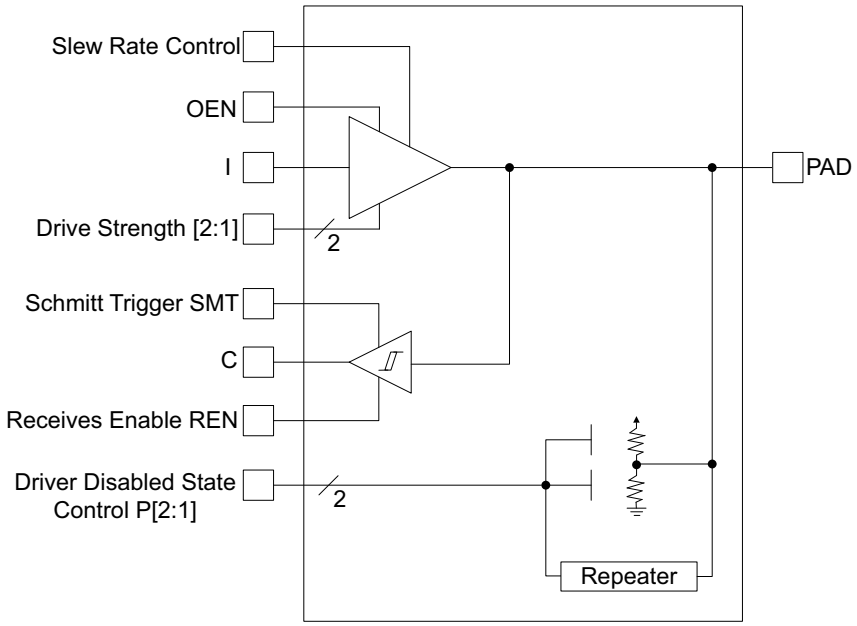

Figure 2.36. : Circuit type TTL

One MSIO cell includes two BIDE33 cells and the PADs are connected to the pins EBP_X and EBN_X (X:0,1). The “Receiver Enable REN” and the “Output Enable OEN” are controlled by the related multiplex function. The remaining ports are controlled by the registers in Table 2.33 .

Table 2.33. : TTL-relevant registers

MSIO TTL Control Ports	MSIO Control Registers
Slew Rate Control	*MSIOCTL_X.ttl_srcn_X* *MSIOCTL_X.ttl_srcp_X* (X:0,1)
Drive Strength [2:1]	*MSIOCTL_X.csn_X* *MSIOCTL_X.csp_X* (X:0,1)
Schmitt Trigger	*MSIOCTL_X.smtn_X* *MSIOCTL_X.smtp_X* (X:0,1)
Drive Disabled State Control P[2:1]	*MSIOCTL_X.ttl_dsn_X* *MSIOCTL_X.ttl_dsp_X* (X:0,1)

Characteristics

- VDE IO supply domain
- CMOS output level

Parameter	Symbol	Min	Typ	Max
High output	VOH	VDE-0.5V		VDE
Low output	VOL	0V		0.5V

- Programmable output drive strength

Drive Setting	Symbol	Min	Typ	Max
00	IOL / IOH	2 ± 1mA		
01	IOL / IOH	4 ± 1mA		
10	IOL / IOH	8 ± 1mA		
11	IOL / IOH	12 ± 12mA		

- CMOS SCHMITT input

Parameter	Symbol	Min	Typ	Max
CMOS	VIH	0.8*VDE		VDE
	VIL	0V		0.2*VDE

- Programmable pull-up/pull-down resistor

Parameter	Symbol	Min	Typ	Max
Pull-up/ pull-down	R	35kOhm	60kOhm	120kOhm

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