Semicustom

CMOS

Standard Cell

CS402 Series

■ DESCRIPTION

The CS402 series of 28 nm standard cells is a line of CMOS ASICs of high-performance with minimum power consumption.

By the adoption of core transistors with high current drivability operating at low voltages, the operating frequency approximately twice that of CS401 series is realized at power supply voltages 10% lower than those of CS401 series.

This series is appropriate for high-performance/high-end applications ranging from the engines of handheld terminals to telecommunication equipment.

■ FEATURES

- Technology : 28 nm Metal-gate CMOS
  : Maximum 11-metal layers. Ultra low permittivity material is used for inter-layer dielectric.
  : Core transistors with different threshold voltages can be used on the same chip (ultra low leak, low leak, standard, high speed and ultra high speed).
- Supply voltage : Internal power supply : + 0.9 V ± 0.09 V
  : External power supply : + 1.8 V ± 0.15 V
  (1.8V interface on dual-power supply system)
- Junction temperature range: – 40 °C to + 125 °C (Standard specification)
- Operating frequency: Approximately twice that of CS401 series
- Support various types of high-quality cell sets developed by SOCIONEXT (from low power versions to high speed versions).
- Support SRAMs with standby-mode and power-down mode for lower power consumption memories.
- Compiled cells (RAM, ROM, others)
- Support special interfaces (LVDS, SSTL, others).
- Support boundary SCAN test.
- Support use of industry standard libraries.
- Support use of industry standard tools.
- Short-term development using a physical prototyping tool
- One-pass design using a physical synthesis tool
- Hierarchical design environment for supporting large-scale circuits
- Support Signal Integrity, EMI noise reduction.
- Support static timing sign-off.
- Improve timing convergence by the introduction of Statistical Static Timing Analysis (SSTA).
- Design For Manufacturing (DFM) enables stable product-supply and reduced variation.
- Package lineup: FBGA, PBGA, TEBGA, FC-BGA

Note: Including items under development.

socionext

■ MACRO LIBRARIES (MACROS CURRENTLY BEING PREPARED ARE INCLUDED)

1. Logic cells (about 400 types)

Library sets for four types of core transistors with different threshold voltages.

- Adder
- AND
- AND-OR
- AND-OR Inverter
- Buffer
- Clock-Buffer
- Delay Buffer
- ENOR
- EOR
- Inverter
- Latch
- NAND
- NOR
- OR
- OR-AND
- OR-AND Inverter
- SCAN Flip flop
- Non-SCAN Flip flop
- Selector
- Others

2. IP macros

CPU/DSP	ARM™* cores (ARM7TDMI-S™*, ARM946E-S™*, ARM926EJ-S™*, ARM1176JZF-S™*, Cortex-M3™*, Cortex-R4F™*, Cortex-A9™* MPCore), Peripherals IP
Mixed signal macro	ADC, DAC,OPAMP, others
Compiled macro	SRAM (1 Port, 2 Port), ROM, product sum calculator, others
PLL	Analog PLL

*: ARM, ARM7TDMI-S, ARM946E-S, ARM926EJ-S, ARM1176JZF-S, Cortex-M3, Cortex-R4F and Cortex-A9 are the trademarks of ARM Limited in the EU and other countries.

3. Special I/O interface macros

Special I/O	LVCMOS, LVDS, SSTL

■ COMPILED CELLS

Compiled cells are macro cells that can be automatically generated by specifying the bit/word configuration. The following compiled cells are available for the CS402 series.

- Memory capacity

Name	Category	Memory capacity (bit)
Clock synchronous single-port RAM (1RW)	High-Density	64 to 1152K
	High-Speed	32 to 80K
	Large-Scale	TBD
Clock synchronous dual port RAM (2RW)	High-Density	32 to 144K
Clock synchronous ROM	—	128 to 1152K
Clock synchronous register file (1RW)	High-Speed	96 to 36K
	High-Density	96 to 36K
Clock synchronous register file (1R1W)	High-Speed	32 to 36K
	High-Density	128 to 72K
Clock synchronous register file (2R2W)	—	16 to 18K

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{DD}	− 0.4	+ 1.3	V	*2
		− 0.5	+ 2.5		*3
Input voltage*1	VI	− 0.5	V_{DD} + 0.5 (≤ 2.5 V)	V	*3
Output voltage*1	VO	− 0.5	V_{DD} + 0.5 (≤ 2.5 V)	V	*3
Storage temperature	T_{STG}	− 55	+ 125	°C	
Junction temperature	Tj	− 40	+ 125	°C	
Output current*4	IO	—	—	mA	
Power supply pin current*5	ID	—	—	mA	

*1: V_{SS} = 0 V

*2: Internal gates

*3: 1.8 V interface on dual-power supply system

*4: The output current varies depending on the number of chip metal layers and the wiring configuration of the I/O cells. For details, contact the sales representative.

*5: For details about the power supply pin current, contact the sales representative.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ DESIGN METHODS

Fujitsu Semiconductor's Reference Design Flow provides the following functions that help reduce the development time of large scale, high quality LSIs.

- Statistical Static Timing Analysis (SSTA) improves timing convergence.
- Physical Prototyping enables more accurate estimation of highly reliable designs.
- Layout synthesis with optimized timing is realized by Physical Synthesis Tool.
- High accuracy design environment where voltage drop of power supply, signal noise, delay penalty and crosstalk are considered
- I/O design environment (power line design, assignment and selection of I/Os, package selection) where noise is considered

■ PACKAGES

The CS402 series can use the same packages that are available for the previous series, allowing a smooth transition from previously developed models. For details of delivery times, contact the sales representative.

- FBGA packages
- PBGA packages
- TEBGA packages
- FC-BGA packages