Data Sheet

MB86R11F
MB86R12
MB86R13

Rev1.00 | December 4, 2018

Socionext Europe GmbH

Graphic Competence Center – GCC

Attached Files

Preface

Intention and Target Audience of this Document

This document describes and gives you detailed insight to the stated Socionext semiconductor product.

The device belongs to the SoCs used for graphics applications.

The target audience of this document is engineers developing products which will use the device. It describes the function and operation of the device. Please read this document carefully.

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Contact Information

For more information on Socionext products or sales inquiries please contact our support team and sales associates through our website www.eu.socionext.com.

History

Version	Date	Comment
1.00	20.11.2018	First release of combined data sheet.

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1 Introduction

The MB86R11F, MB86R12 and MB86R13 devices are System-on-chip (SoC) solutions that incorporate an ARM Cortex A9 CPU and the Socionext's Graphic Display Controller (GDC) MB86298 as its core. The MB86R11F/12/13 implements an LSI-architecture that contains peripheral I/O resources, such as in-vehicle LAN, HDD, etc. in a single chip solution. Many graphics solutions using only a single chip, where previously more complex and costly solutions using two separate chips, CPU and GDC, were required, are now possible.

Table 1.1 summarizes the differences between devices MB86R11F, MB86R12 and MB86R13.

Table 1.1. : MB86R11F/12/13 specifications

	MB86R11F	**MB86R12**	**MB86R13**
Package	PBGA	TEBGA	TEBGA
APIX	No	Yes	No
USB2.0	Yes	No	No
DDR	DDR3-800 DDR2-800/667	DDR3-1066/800 DDR2-800/667	DDR3-1066/800 DDR2-800/667
Clock	CPU:400MHz AXI:200MHz AHB:100MHz APB:50MHz	CPU:533MHz AXI:266MHz AHB:133MHz APB:66MHz	CPU:533MHz AXI:266MHz AHB:133MHz APB:66MHz

Technology

- CMOS 65nm
- Power supply voltage: 3.3 ±0.3V (IO), 1.2 ±0.1V (core), 1.5 ±0.1V (DDR3), 1.8 ±0.1V (DDR2)

Package

- MB86R11F: PBGA-544
- MB86R12, MB86R13: TEBGA-544
- Ambient temperature range: -40 … +85°C

Memory Interface

- MB86R11F: 32-bit DDR3-800 / DDR2-800
  - 32-bit/16-bit width mode (half of data pins are not used in 16-bit mode)
- MB86R12/13: 32-bit DDR3-800 / DDR3-1066 / DDR2-800/DDR2-667
  - 32-bit/16-bit width mode (half of data pins are not used in 16-bit mode)

1.1. Key Features

- CPU Core (ARM Cortex-A9)
- Bus architecture: Multi-layer AXI/AHB/APB bus architecture
- Interrupts
- Built-in SRAM
- Clock/Reset Control
- General Purpose External Bus (32bit/16bit)

- Unified 16-bit / 32-bit DDR3/DDR2 memory interface
- GDC - Graphics Display Controller
- SDIO/MMC - Memory Controller (CPRM: not supported) x 3 channels
- ADC - 12-bit Analog/Digital Converter (500 kS/s) x 2 channels
- I^2C - Inter-Integrated Circuit - I/O voltage: 3.3V x 5 channels
- CAN - Controller Area Network (I/O voltage: 3.3V) x 2 channels
- MediaLB - Media Local Bus (3-pin) x 1 channel
- USART/UART - Universal Synchronous/Asynchronous Receiver Transmitter x 6 channels
- GPIO - General Purpose Input/Output x 128bit
- SFI/SPI - Serial Flash Interface x 2 channels
- HS-SPI - High-speed Serial Peripheral Interface x 1 channel
- I^2S - Serial Audio Interface x 4 ports (2 channels/port)
- PWM - Pulse Width Modulator x 12 channels
- IrDA - Infrared Data Transfer (Ver.1.0) x 1 channel
- TS - Transport Stream Interface x 1 channel
- 32-/16-bit timer x 2 channels
- DMAC - Direct Memory Access Controller x 16 channels
- SIG - Signature Unit x 3 channels
- Ethernet link x 1 channel
- IDE66 (ATA/ATAPI-5) x 1 channel
- RLD - Run-length decompression
- Embedded TCON - Timing controller function
- Host interface
- USB 2.0 Host/Function x 1 channel, USB 2.0 Host x 1 channel
- APIX (Tx 3 channels, Rx 1 channel - only in MB86R12)
  Note: See Limitation of the APIX Interface below.

Restrictions

- The DDR2/3 controller does not support small size WRAP burst (16bytes or less).
  Please replace it with INCR burst transfer or SINGLE transfer when you want to transfer 32-bit WRAP4 DMAC.
- GPIO peripheral mode is not supported.
- HDMAC external DMA request is not supported (only peripheral DMA requests are supported).
- 8-bit SRAM and 8-bit NOR Flash are not supported by the External Bus Controller (8-bit NAND Flash is supported).
- External interrupt#3 signal is internal clipped. 7 external interrupts can be used (0-2, 4-7).
- UART flow function supports only channela 0-3 (channels 4 and 5 are not supported).
- The ethernet controller Tr/Tf characteristic specification at C_load 5pf is 1.50ns, which does not comply to the GMII specification. Therefore, the system designer should implement the buffer on the PCB in some other way in order to fulfill the Tr/Tf specification.
- SFI0_HOLD can use only SFI 1(Pix multiplex #B).
- Limitations of the APIX Interface:
  When I2S is connected with APIX2TX, the following registers cannot be used. (I2S master mode): CNTREG.SMPL, CNTREG.RXDIS, CNTREG.BEXT, OPRREG.RXENB INTCNT.RFTH - INTCNT.RPTMR INTCNT.RXFIM, INTCNT.RXFDM, NTCNT.EOPM, INTCNT.RXOVM,

INTCNT.RXUDM, INTCNT.RBERM, INTCNT.FERRM, STATUS.RXNUM, STATUS.RXFI, STATUS.EOPI, STATUS.RXOVR, STATUS.RXUDR, STATUS.FERR, STATUS.TBERR, DMAACT.RDMACT, DMAACT.RL1E0

When I2S is connected with APIX2RX, the following registers cannot be used. (I2S slave mode):
CNTREG.FSLN, CNTREG.TXDIS, CNTREG.FRUN, CNTREG.ECKM, CNTREG.MSKB, CNTREG.OVHD, CNTREG.CKR, OPRREG.TXENB, NTCNT.TFTH, INTCNT.TXFIM, INTCNT.TXFDM, INTCNT.TXOVM, INTCNT.TXUD0M, INTCNT.TBERM, INTCNT.TXUD1M, STATUS.TXNUM, STATUS.TXFI, STATUS.BSY, STATUS.TXOVR, STATUS.TXUDR0, STATUS.TXUDR1, STATUS.RBERR, DMAACT.TDMACT, DMAACT.TL1E0
Please set the value of the CNTREG.ECKM register according to the value of the APIXCTL.I2S_CKSELregister of CCNT when you connect I2S with APIX2TX.

The herein integrated APIX2 Transmitters are not compliant to the APIX2 Requirement Specification and Functionality Specification, max cable length in 3Gb/s mode is limited to 1.5m.

1.2. Block Diagrams

The functional figures show the functional blocks of MB86R11F/12/13 devices.

1.2.1. MB86R11F Block Diagram

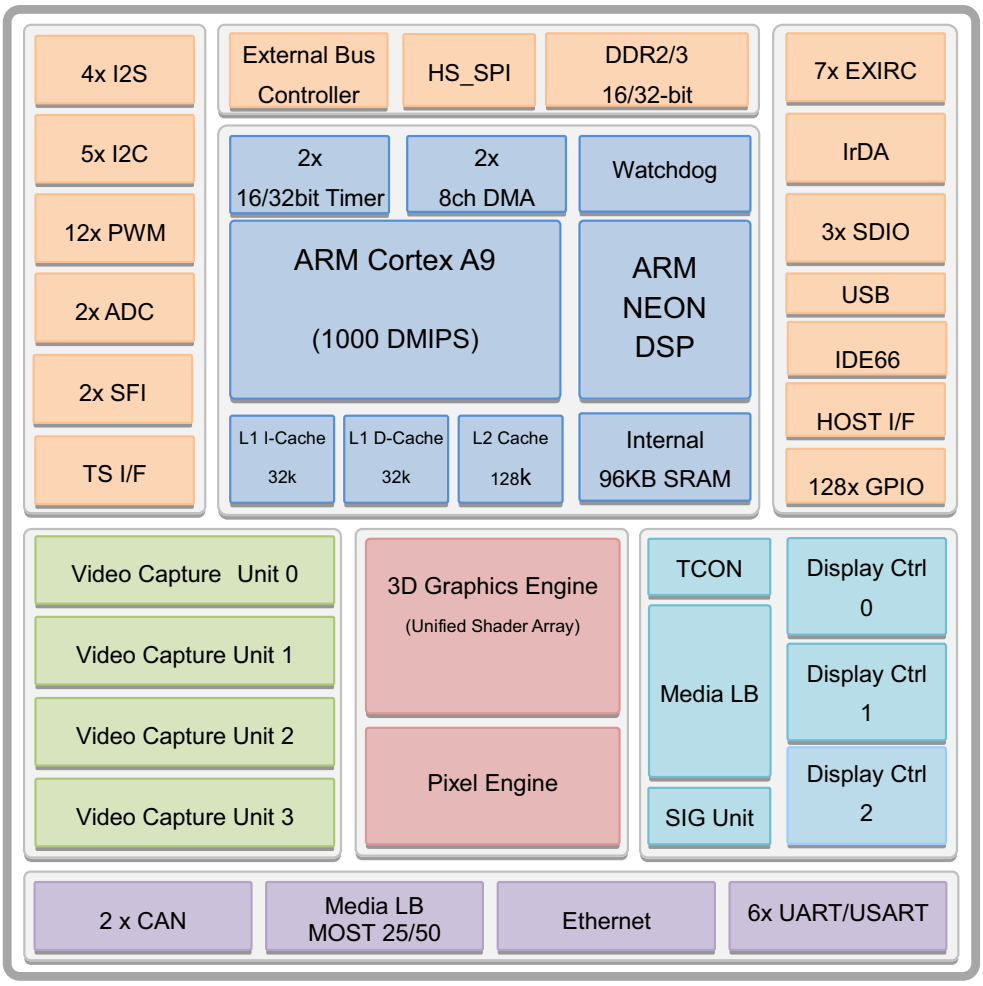


Figure 1.1. : MB86R11F block diagram

1.2.2. MB86R12 Block Diagram

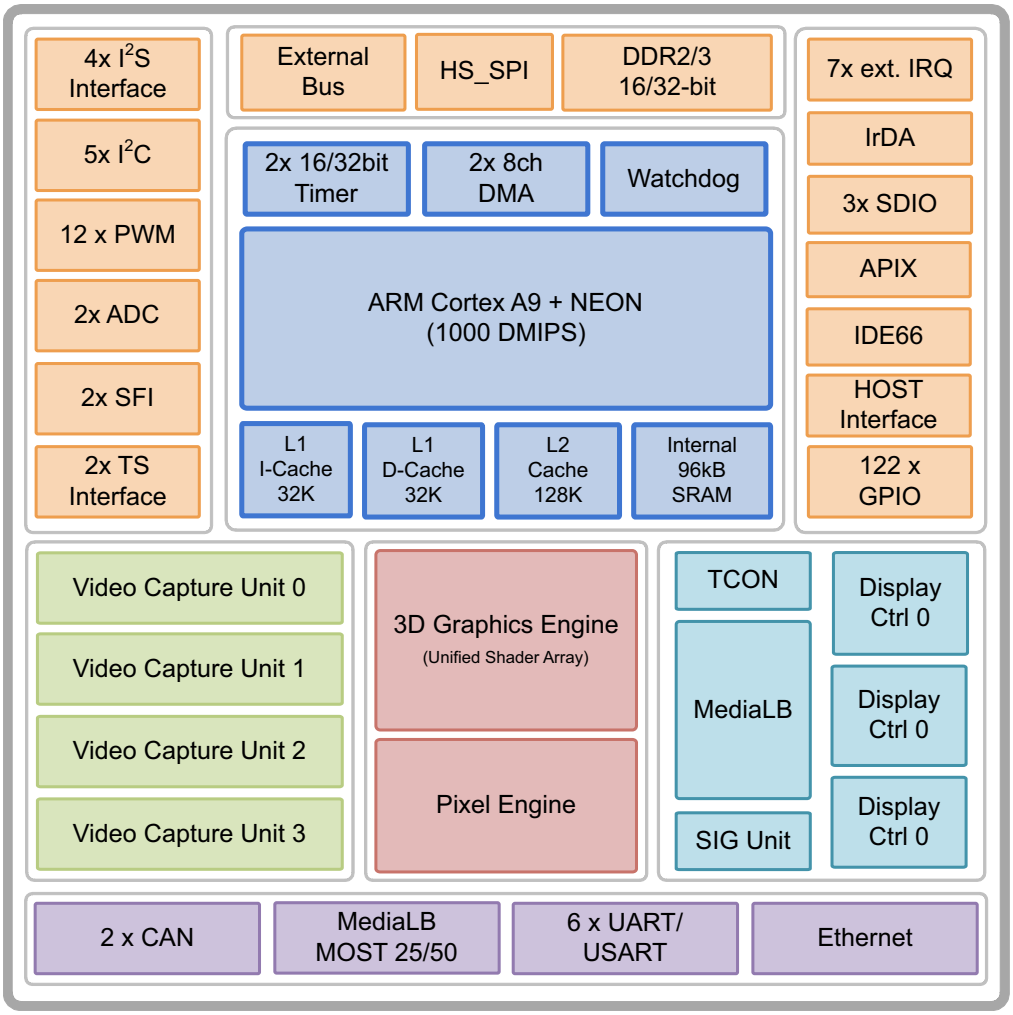


Figure 1.2. : MB86R12 block diagram

1.2.3. MB86R13 Block Diagram

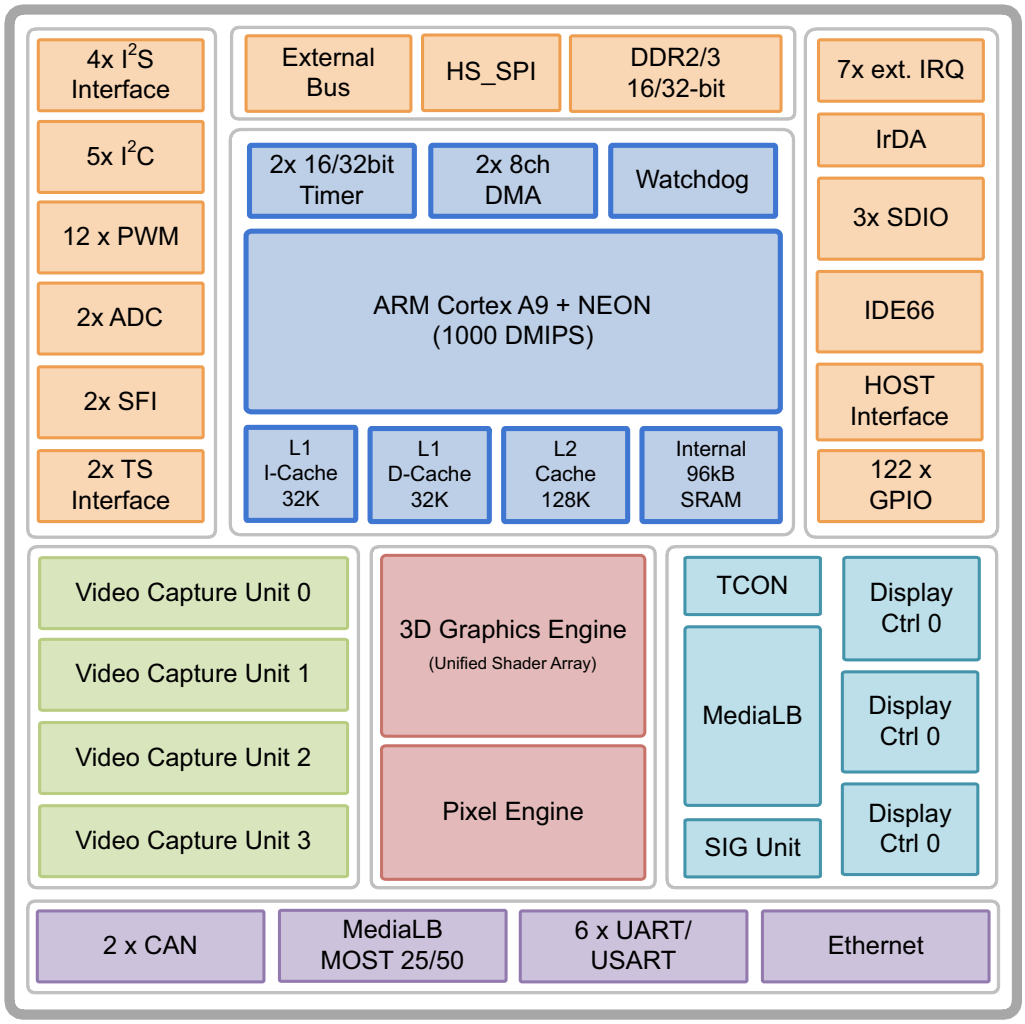


Figure 1.3. : MB86R13 block diagram

1.3. Outline of Each Functional Block

AXI0 Bus (64bit)

- Cortex A9
- Video Capture Unit x 4
- Display Unit x 3
- Write Back Unit
- 3D Graphics Engine
- Pixel Engine
- Command Sequencer x 2
- DDR2/DDR3 Controller
- AXI-DMA Controller (XDMAC) 8 channels

- Built-in SRAM (XSRAM) 32kB
- External Bus Controller
- IrDA
- TS Interface

AHB0 Bus (32bit)

- USB 2.0 HOST
- USB 2.0 HOST/FUNC
- SDIO x 3
- MediaLB
- Built-in SRAM (HSRAM) 32kB
- Boot ROM 64kB
- HOST Interface

AHB1 Bus (32bit)

- IDE66
- Ethernet Link
- Watchdog Timer B
- Built-in SRAM (HSRAM) 32kB
- AHB-DMA controller (HDMAC) 8channels
- Run-length Decompression (RLD)
- SFI x 2
- I2S x 4

AHB2 Bus (32bit)

- SIG x 3
- Display Controller 2 (register access)
- Command Sequencer (register access)
- Pixel Engine (register access)
- DDR Memory Controller (register access)
- TCON
- HS_SPI
- APIX (Tx 3ch, Rx 1ch)

APB0 Bus (32bit)

- UART/USART x 6
- Timers 32bit/2 channels
- Watchdog Timer A
- External Interrupt Controller 3 channels x 1; 4 channels x 1
- Boot Controller
- GPIO 128 channels
- Clock Reset Generator S (for SSCG)
- Clock Reset Generator P (for non SSCG)

- External Bus Controller (register access)
- PWM (4 channels) x 3
- A/D Converter x 2
- CCNT
- I^2C x 5
- CAN x 2
- Power Management Unit

1.4. System Configuration

The following diagrams show an overview of the system configuration.

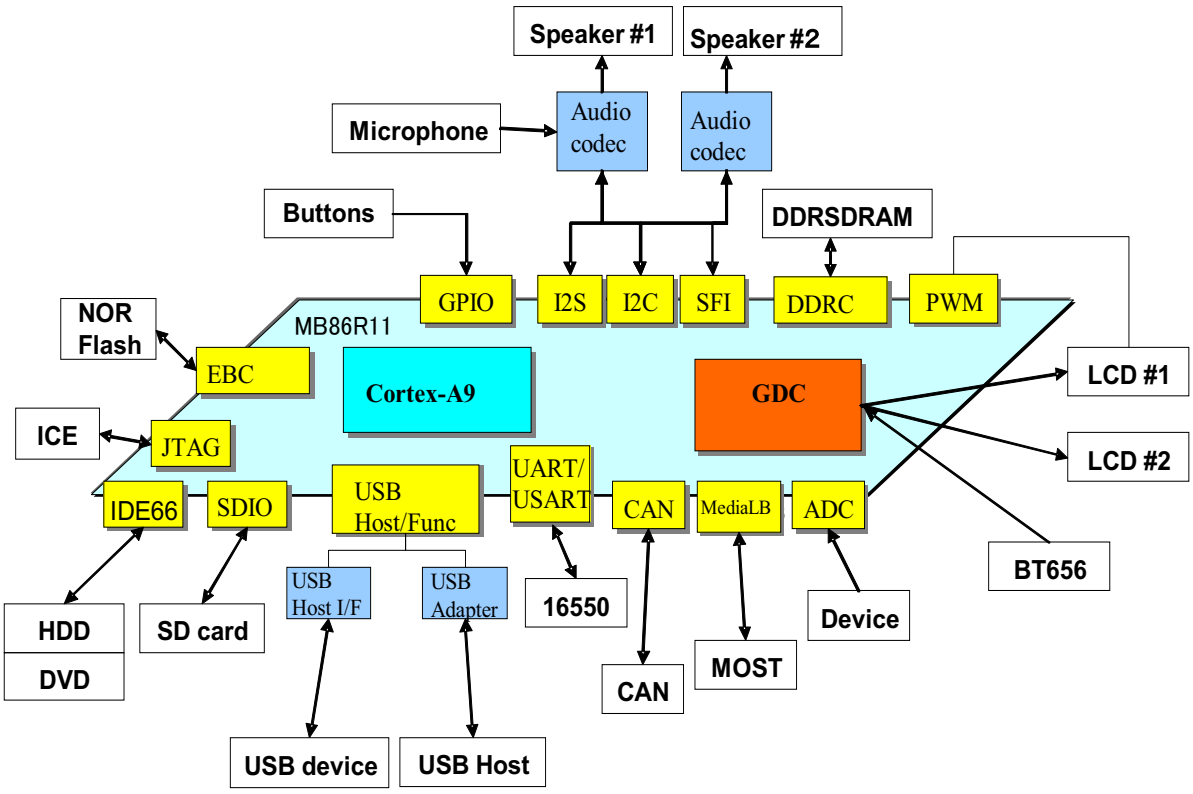


Figure 1.4. : MB86R11F system configuration

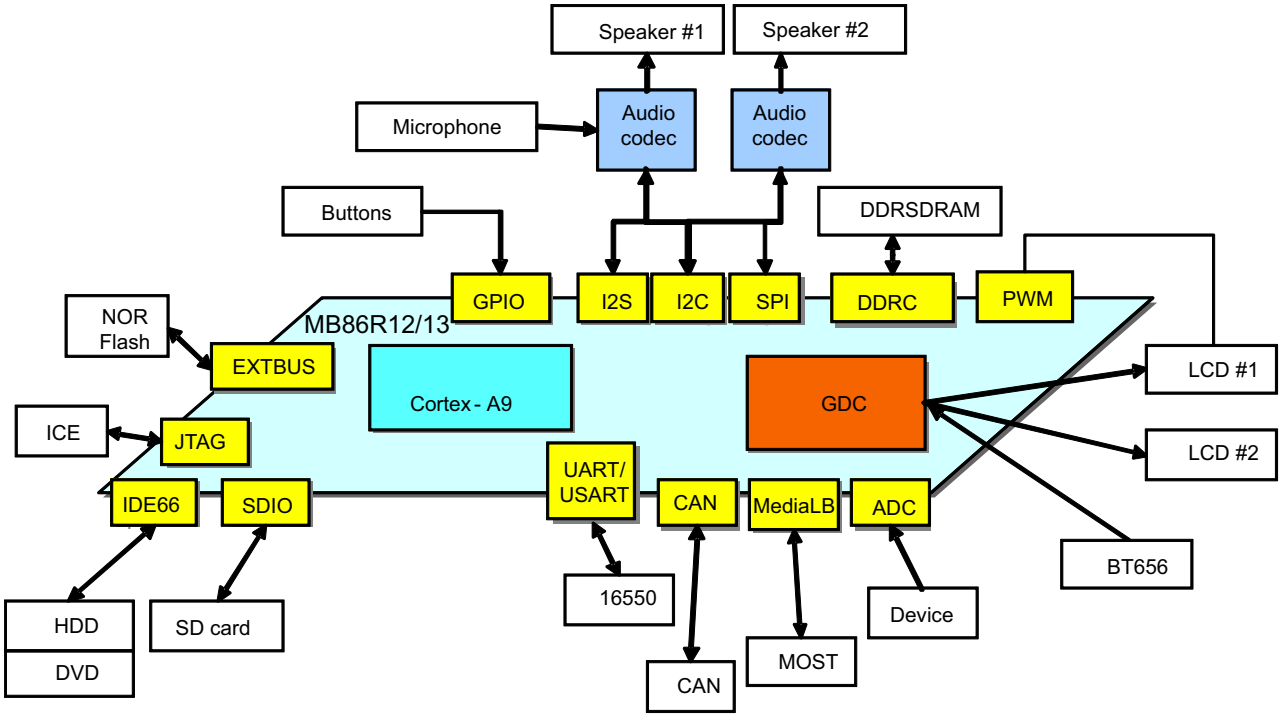


Figure 1.5. : MB86R12/13 system configuration

1.5. Function List

Table 1.2 shows the function list of the MB86R11F/12/13.

Table 1.2. : Function list

Functions	Description
CPU core	- ARM Cortex A9™ processor core - Core operation frequency: MB86R11F: 400MHz; MB86R12/13: 533MHz - 32kB instruction cache - 32kB data cache - PTM and JTAG ICE debugging interface - Java acceleration (Jazelle technology)
Bus architecture	- Multilayer AXI/AHB/APB bus architecture
Interrupt	- Software Generated interrupt x 16 channels - External interrupt x 7channels - Internal interrupts
Clock	- Operation frequency MB86R11F: 400MHz (CPU), 200MHz (AXI), 100MHz (AHB), 50MHz (APB) MB86R12/13: 533MHz (CPU), 266MHz (AXI), 133MHz (AHB), 66MHz (APB) - Low power consumption mode (clock to block is stoppable)
Reset	- Hardware reset, software reset, and watchdog reset
External bus controller	- Three chip select signals - Provided 128Mbyte address space in each chip select (Max 256Mbyte) - Supported 16/32-bit width SRAM/NOR Flash - Supported 8/16-bit width NAND Flash - Programmable weight controller
DDR3/DDR2 controller	- Supported: DDR3SDRAM (MB86R11F: DDR3-800; MB86R12/13: DDR3-800/1066) DDR2SDRAM (MB86R11F: DDR2-800/667; MB86R12/13: DDR2-800/667) - Connectable capacity: 2048Mbit ~ 4096Mbit x 2 or 2048Mbit ~ 4096Mbit x 1 - I/O width: Selectable from x16/x32bit - Max. transfer rate: MB86R12/13: DDR3 533MHz/1066Mbps, DDR2 400MHz/800Mbps MB86R11F: 400MHz/800Mbps
Internal SRAM	- Mounted general purpose SRAM of 32kB x 2 on AHB (32-bit bus) - Mounted general purpose SRAM of 32kB x 1 on AXI (64-bit bus)
DMAC	- AHB connection x 8 channels - AXI connection x 8 channels - Transfer mode: Block, burst, and demand
Timer	- 32/16-bit programmable x 2 channels
GPIO	- Max 128bit
PWM	- Internal 12 channels - Duty ratio and phase are configurable
A/D converter	- 12bit successive approximation type A/D converter x 2 channels - Sampling rate: 500kS/s (max. sampling plate) - INL: ± 4.0LSB, DNL: ± 4.0LSB

Table 1.2. : Function list (Continued)

Functions	Description
Capture/Display Controller	- GDC (graphic display controller) has role of display and capture. Two main display controllers and one simplified display controller are available. The two main display controllers can show up to 8 different layers whereas the simplified can show 1 layer. Four video capture controllers with crossbar switch can capture four independent video sources with flexibility. **Note**: Simultaneous usage of these function depends on available SDRAM bandwidth and pin multiplex mode.
3D Graphics Engine	- OpenGL ES2.0 compliant. - Support for 2D concave polygon. - Support for Anti-aliased lines. - Support for 16/32-bit color format. - Support for 32-bit RGBA/ABGR/ARGB frame buffer or texture format. - Support for 8/16/32-bit depth buffer format.
Pixel Engine	- Pixel processing units used for block image transfer (blt) operations to a memory.
I^2S	- Audio output x 4 channels (L/R) /Audio input x 4 channels (L/R) - Supported three-wire serial (I^2S, MSB-Justified) and serial PCM data transfer interface - Master/Slave operations are selectable - Resolution capability: Max. 32bit/sample
UART/USART	- Max. 6 channels - 4 channel: capable of input/output CTS/RTS signals - Enabled DMA transfer
I2C	- 3.3V pin x 5 channels - Supported standard mode (max. 100kbps)/high-speed mode (max. 400kbps) - Master/Slave operations are selectable
SFI	- 2 channels - Full duplex/Synchronous transmission - Transfer data length: 1bit unit (max. 32bit) (programmable setting)
CAN	- Mounted BOSCH C_CAN module 2 channels - Conformed to CAN protocol version 2.0 part A and B - I/O voltage: 3.3V
MediaLB	- 16 hardware channels - MediaLB clock speed: 256Fs/512Fs/1024Fs - Internal 9kbit channel buffer
IDE	- Supported ATA/ATAPI-5 - Equipped 1 channel - Supported primary IDE channel - Equipped transmission FIFO buffer (512byte x 2) and reception FIFO buffer (512byte x 2) for the ultra DMA transfer - Unsupported single word DMA and multi word DMA
SD memory	- Conformed to SD memory card physical layer specification 1.0 - Equipped 3 channel - Supported SD memory card and multimedia card - Unsupported SPI mode and CPRM
CCNT	- Chip General Control

Table 1.2. : Function list (Continued)

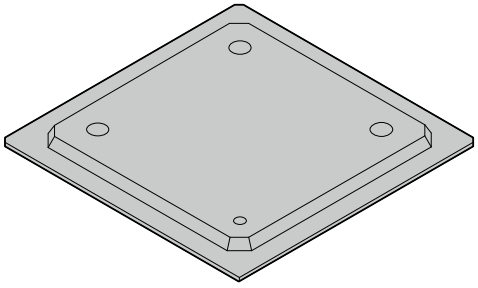
Functions	Description
IrDA	- IrDA 1.0 SIR (2.4k – 115.2kbps) - IrDA 1.1 MIR (0.576Mbps or 1.152Mbps) - IrDA 1.1 FIR (4.0Mbps) - 32 step x 2 transmitting and receiving FIFO
SIG	- 3 channels - Generation of 2 different picture signatures for each color channel: - Summation of color values - CRC-32 over color values - Programmable evaluation window position and size - Programmable evaluation window mask - Automatic monitoring using reference signature registers - Interrupt generation - Programmable picture source - Self restoring error counter
Ethernet	- Compliant with IEEE802.3 specification - Supports 10/100/1000Mbps data transfer rates - Supports 10/100/1000Mbps Full-Duplex and Half-Duplex modes - IEEE802.3 GMII and MII interfaces
TCON	- RBM (RSDS Bit Mapping) Conforms to RSDS™ Standard 1.0 (National Semiconductors) Support for single bus (Multidrop bus with single or double end termination) Mapping for 8bit color depth Data and clock outputs can flexible be assigned to the pool of available pins to ease board design - TSIG (Timing Signal Generator) Freely programmable waveforms 12 pulse generators 1 signal sequencer with max. 64 signal transitions 12 signal mixers with a programmable function table Inversion control signal for transition minimizing (useful for TTL applications) - IO module Output RGB data Control of Combined TTL/RSDS IO cells Output RSDS clock Output TTL clock 90° phase shift - Adjustable differential swing

Table 1.2. : Function list (Continued)

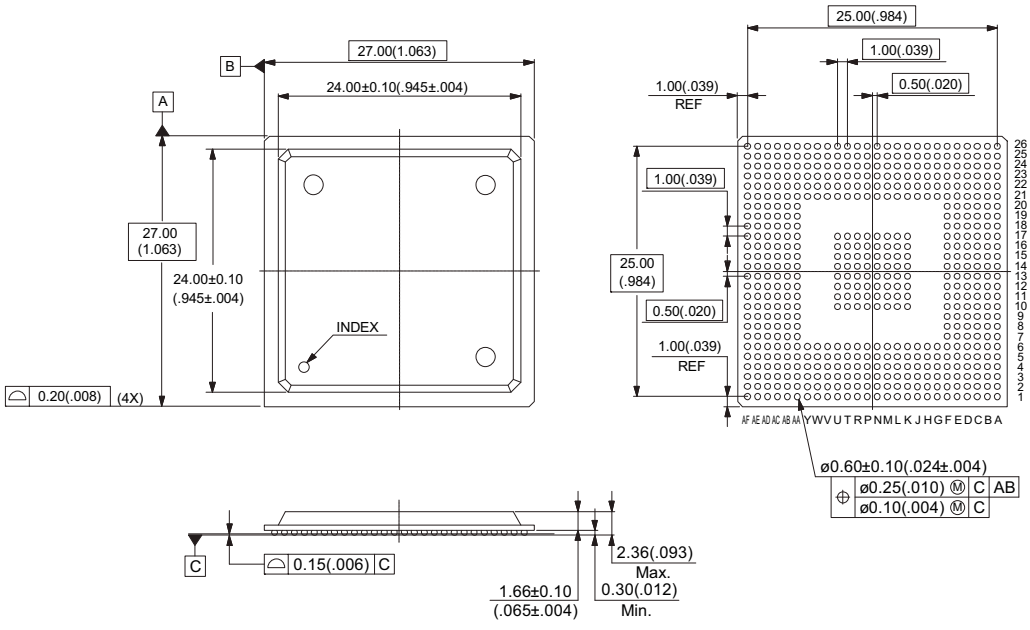
Functions	Description
USB	- Function Link and Host Link combined with one PHY - Host Link with one PHY - Built in DMAC only for Function Link - Function Link has ControlOut/In Endpoint, Bulk In/Out Endpoint, Interrupt In Endpoint - Function Link contains 64byte buffer for Control Endpoint, 512byte x 2 buffer for Bulk Endpoint, 64byte buffer for Interrupt Endpoint - Contains a controller supporting both the EHCI and OHCI - Handles the USB2.0 HS, FS and LS protocols - Host Link contains 512bytes of packet buffers Note: USB only in MB86R11F
RLD	- Support of simple run-length compression format (TGA™ similar format) - 8/16/24/32-bit per pixel formats supported - AHB master for data output - FIFO for data input and output, allows burst access of AHB
TS	- 2 serial TS input channels and 1 parallel (8bit) TS input channel are supported. - The TSD interface supports serial mode input rate up to 66Mbit/s. Parallel mode input rate up to 20Mbit/s.
HOST Interface	- Supports communication to a host CPU.
HS_SPI	- Supports legacy as well as the dual-bit and quad-bit modes of SPI operation - Up to 4 slave devices
Watchdog Timer	- 3 Watchdog timers: WDT A, WDT B, Cortex-A9 Internal WDT
PMU	- Controls power switch transistor in LSI to reduce power consumption. - Power supply On/Off control and the interrupt of an unused block.
APIX	- The APIX2RX_link for the MB86R12 links the different APIX2RX interfaces to the bus system and to the capture units. Note: APIX only in MB86R12.
JTAG	- Conformed to IEEE1149.1 (IEEE Standard Test Access Port and Boundary-Scan Architecture) - Supported JTAG ICE connection
Note: Number of layer of simultaneous display and number of output display as well as capture input for displaying in high resolution may be restricted due to data supply capacity of graphics memory (DDR Memory controller).	

1.6. Package

1.6.1. MB86R11F Package

544-pin plastic PBGA		
	Lead pitch	1.00 mm
	Package width × package length	27.00 mm × 27.00 mm
	Lead shape	Ball
	Sealing method	Plastic mold
	Mounting height	2.36 mm MAX
	Weight	2.80 g
(BGA-544P-M04)		

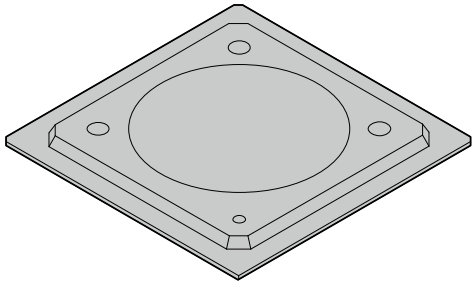
544-pin plastic PBGA
(BGA-544P-M04)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

1.6.2. MB86R12/13 Package

The MB86R12/13 is provided in a thermally enhanced ball grid array (TEBGA) package with 544 balls.

544-pin plastic TEBGA		
	Lead pitch	1.00 mm
	Package width × package length	27.00 mm × 27.00 mm
	Lead shape	Ball
	Sealing method	Plastic mold
	Mounting height	2.36 mm MAX
	Weight	3.70 g
(BGA-544P-M02)		

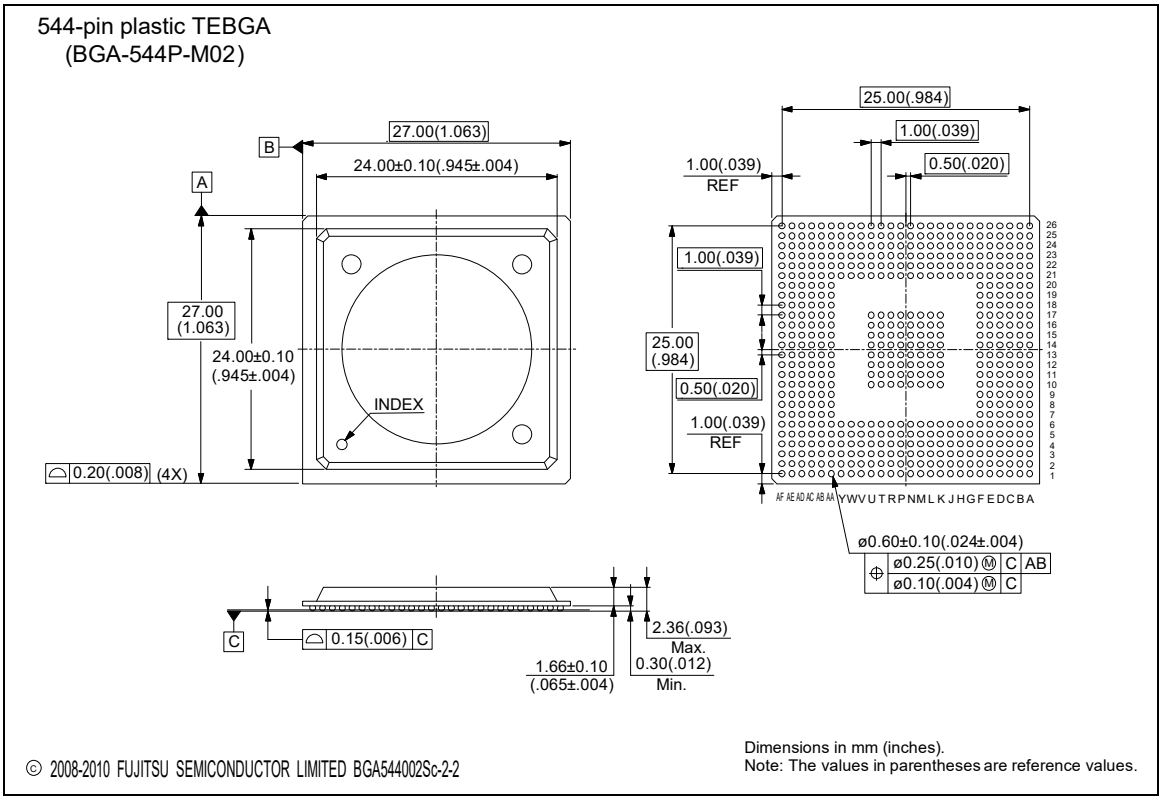


Figure 1.6. : TEBGA-544 Package dimensions

Note: The contents of this figure are subject to change without notice. Customers are advised to consult with Socionext sales representatives before ordering. Socionext Europe GmbH is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of the information or package dimensions in this document.

1.7. Device Handling

1.7.1. Latch-Up

If a voltage higher than VDD or a voltage lower than VSS are applied to an input and/or output pin of a CMOS IC, a so-called 'latch-up' phenomenon could occur. In this case, the power supply current might increase suddenly, leading to the thermal destruction of the device.

Note: Do not exceed the maximum ratings.

1.7.2. Unused Pin

If an input pin is not used, apply a pull-up or pull-down resistor as specified to avoid the permanent destruction of the device due to the latch-up phenomenon, caused by high resistance.

1.7.3. Power Supply Pin

Connect all VDD/VSS pins to the same power supply. Otherwise the device will not work correctly, not even in the guaranteed operating range.

1.7.4. Oscillation Circuit

Noise will affect the XTAL_XI and XTAL_XO external pins, leading to malfunction. Therefore, the oscillator and its bypass capacitor should be placed near to the device's XTAL_XI/XTAL_XO pins.

The surroundings of these pins require carefully grounding.

1.7.5. Attention PLL Clock's Working

If the external clock stops, the device might continue operating at the same frequency of the internal PLL-oscillator. This operation is outside the guaranteed operation range.

1.8. Pinning

1.8.1. Pin Assignment

The following diagram shows the pin-out assignment of the MB86R11F/12/13.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	1	100	99	98	97	96	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80	79	78	77	76	A
B	2	101	192	191	190	189	188	187	186	185	184	183	182	181	180	179	178	177	176	175	174	173	172	171	170	75	B
C	3	102	193	276	275	274	273	272	271	270	269	268	267	266	265	264	263	262	261	260	259	258	257	256	169	74	C
D	4	103	194	277	352	351	350	349	348	347	346	345	344	343	342	341	340	339	338	337	336	335	334	255	168	73	D
E	5	104	195	278	353	420	419	418	417	416	415	414	413	412	411	410	409	408	407	406	405	404	333	254	167	72	E
F	6	105	196	279	354	421	480	479	478	477	476	475	474	473	472	471	470	469	468	467	466	403	332	253	166	71	F
G	7	106	197	280	355	422															465	402	331	252	165	70	G
H	8	107	198	281	356	423															464	401	330	251	164	69	H
J	9	108	199	282	357	424															463	400	329	250	163	68	J
K	10	109	200	283	358	425				481	508	507	506	505	504	503	502				462	399	328	249	162	67	K
L	11	110	201	284	359	426				482	509	528	527	526	525	524	501				461	398	327	248	161	66	L
M	12	111	202	285	360	427				483	510	529	540	539	538	523	500				460	397	326	247	160	65	M
N	13	112	203	286	361	428				484	511	530	541	544	537	522	499				459	396	325	246	159	64	N
P	14	113	204	287	362	429				485	512	531	542	543	536	521	498				458	395	324	245	158	63	P
R	15	114	205	288	363	430				486	513	532	533	534	535	520	497				457	394	323	244	157	62	R
T	16	115	206	289	364	431				487	514	515	516	517	518	519	496				456	393	322	243	156	61	T
U	17	116	207	290	365	432				488	489	490	491	492	493	494	495				455	392	321	242	155	60	U
V	18	117	208	291	366	433															454	391	320	241	154	59	V
W	19	118	209	292	367	434															453	390	319	240	153	58	W
Y	20	119	210	293	368	435															452	389	318	239	152	57	Y
AA	21	120	211	294	369	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	388	317	238	151	56	AA
AB	22	121	212	295	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	316	237	150	55	AB
AC	23	122	213	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	236	149	54	AC
AD	24	123	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	148	53	AD
AE	25	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	52	AE
AF	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	AF

Figure 1.7. : Top view of the pin assignment (pin number)

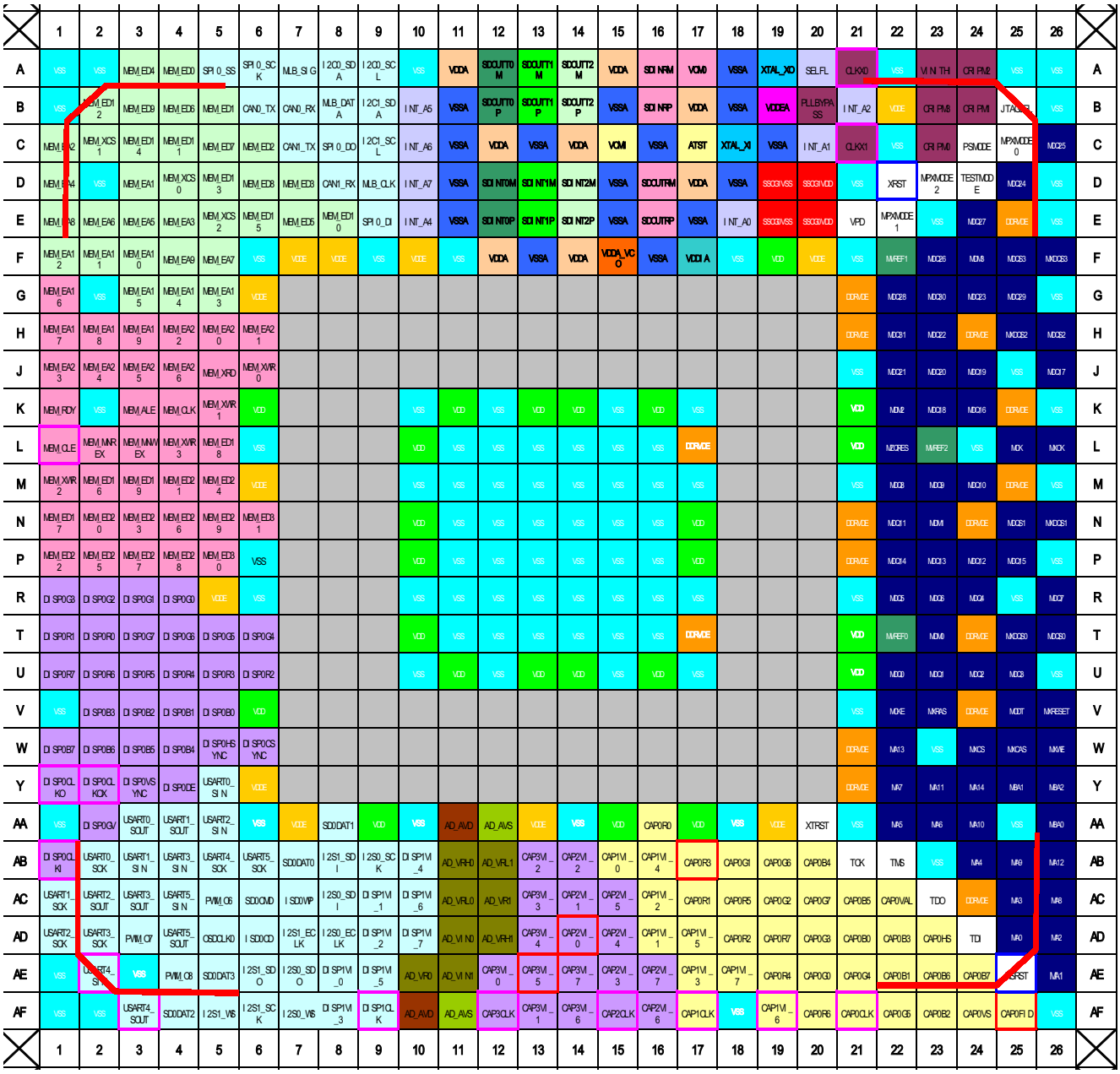
1.8.2. Functional Pin Assignment

1.8.2.1. MB86R11F Pin Assignment

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26		
A		VSS	VSS	MEM_EA24	MEM_EA21	MEM_EA17	MEM_EA13	MEM_EA8	MEM_EA7	MEM_EA2	MEM_ED15	MEM_ED13	MEM_ED8	MEM_ED5	MEM_ED1	CAN1_TX	SPI0_DI	TEST	TEST	TEST	SELFL	CLKX0	VSS	VINITHI	CRIPM2	VSS	VSS		A
B		VSS	MEM_CLK	MEM_XRD	MEM_EA23	MEM_EA18	MEM_EA14	MEM_EA9	MEM_EA3	MEM_EA1	VSS	MEM_ED11	MEM_ED6	MEM_ED2	VSS	SPI0_SCK	SPI0_DO	TEST	TEST	TEST	INT_A1	PLLBYPASS	VDDE	CRIPM3	CRIPM1	JTAGSEL	VSS		B
C		MEM_XWR2	VSS	MEM_RDY	MEM_EA25	MEM_EA20	MEM_EA15	MEM_EA10	MEM_EA4	MEM_XCS2	MEM_ED14	MEM_ED9	MEM_ED4	CAN1_RX	SPI0_SS	MLB_CLK	I2C1_SCL	INT_A7	TEST	INT_A2	INT_A0	CLKX1	VSS	CRIPM0	PSMODE	MPXMODE0	MDQ25		C
D		MEM_ED17	MEM_ED16	MEM_XWR1	MEM_XWR0	MEM_EA22	MEM_EA16	MEM_EA11	MEM_EA6	MEM_XCS1	MEM_ED12	MEM_ED7	MEM_ED0	CAN0_TX	MLB_SIG	I2C0_SDA	INT_A6	TEST	TEST	SSCG1VSS	SSCG1VDD	VSS	XRST	MPXMODE2	TESTMODE	MDQ24	VSS		D
E		MEM_ED22	MEM_ED18	MEM_XWR3	MEM_CLE	MEM_EA26	MEM_EA19	MEM_EA12	MEM_EA5	MEM_XCS0	MEM_ED10	MEM_ED3	CAN0_RX	MLB_DATA	I2C0_SCL	INT_A5	INT_A4	TEST	TEST	SSCG0VSS	SSCG0VDD	VPD	MPXMODE1	VSS	MDQ27	DDRVDE	VSS		E
F		MEM_ED26	MEM_ED23	MEM_ED19	MEM_MNWEX	MEM_ALE	VSS	VDDE	VDDE	VSS	VDD	VDD	I2C1_SDA	VDDE	VSS	VDD	TEST	TEST	VSS	VDD	VDDE	VSS	MVREF1	MDQ26	MDM3	MDQS3	MXDQS3		F
G		MEM_ED29	MEM_ED27	MEM_ED24	MEM_ED21	MEM_MNREX	VDDE															DDRVDE	MDQ28	MDQ30	MDQ23	MDQ29	VSS		G
H		USB0_CRYCK48	VSS	MEM_ED31	MEM_ED30	MEM_ED28	VDD															DDRVDE	MDQ31	MDQ22	DDRVDE	MXDQS2	MDQS2		H
J		USB0_DP	USB0_AVSF	USB0_SYSINT	USB0_OC	MEM_ED25	MEM_ED20															VSS	MDQ21	MDQ20	MDQ19	VSS	MDQ17		J
K		USB0_DM	USB0_AVSF	USB0_AVDP	USB0_AVSP	USB0_PRTPWR	VSS				VSS	VDD	VSS	VDD	VDD	VSS	VDD	VSS				VDD	MDM2	MDQ18	MDQ16	DDRVDE	VSS		K
L		USB1_DM	USB1_AVSF	USB0_AVDF2	USB0_AVDF1	USB0_AVDB	USB0_AVSB				VDD	VSS	VSS	VSS	VSS	VSS	VSS	DDRVDE				VDD	MZQRES	MVREF2	VSS	MCK	MXCK		L
M		USB1_DP	USB1_AVSF	USB1_AVDF1	USB1_AVDF2	USB0_AVSF	USB0_EXT12K				VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS				VSS	MDQ8	MDQ9	MDQ10	DDRVDE	VSS		M
N		USB1_CRYCK48	USB1_OC	USB1_AVDP	USB1_AVSP	USB1_AVDB	USB1_AVSF				VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD				DDRVDE	MDQ11	MDM1	DDRVDE	MDQS1	MXDQS1		N
P		USB1_PRTPWR	VSS	USB1_SYSINT	VSS	USB1_AVSB	USB1_EXT12K				VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD				DDRVDE	MDQ14	MDQ13	MDQ12	MDQ15	VSS		P
R		DISP0G3	DISP0G2	DISP0G1	DISP0G0	VDDE	VSS				VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS				VSS	MDQ5	MDQ6	MDQ4	VSS	MDQ7		R
T		DISP0R1	DISP0R0	DISP0G7	DISP0G6	DISP0G5	DISP0G4				VDD	VSS	VSS	VSS	VSS	VSS	VSS	DDRVDE				VDD	MVREF0	MDM0	DDRVDE	MXDQS0	MDQS0		T
U		DISP0R7	DISP0R6	DISP0R5	DISP0R4	DISP0R3	DISP0R2				VSS	VDD	VSS	VDD	VDD	VSS	VDD	VSS				VDD	MDQ0	MDQ1	MDQ2	MDQ3	VSS		U
V		VSS	DISP0B3	DISP0B2	DISP0B1	DISP0B0	VDD															VSS	MCKE	MXRAS	DDRVDE	MODT	MXRESET		V
W		DISP0B7	DISP0B6	DISP0B5	DISP0B4	DISP0HSYNC	DISP0CSYNC															DDRVDE	MA13	VSS	MXCS	MXCAS	MXWE		W
Y		DISP0CLKO	DISP0CLKOX	DISP0VSYNC	DISP0DE	USART0_SIN	VDDE															DDRVDE	MA7	MA11	MA14	MBA1	MBA2		Y
AA		VSS	DISP0GV	USART0_SOUT	USART1_SOUT	USART2_SIN	VSS	VDDE	SD0DAT1	VDD	VSS	AD_AVD	AD_AVS	VDDE	VSS	VDD	CAP0R0	VDD	VSS	VDDE	XTRST	VSS	MA5	MA6	MA10	VSS	MBA0		AA
AB		DISP0CLKI	USART0_SCK	USART1_SIN	USART3_SIN	USART4_SCK	USART5_SCK	SD0DAT0	I2S1_SDI	I2S0_SCK	DISP1VI_4	AD_VRH0	AD_VRL1	CAP3VI_2	CAP2VI_2	CAP1VI_0	CAP1VI_4	CAP0R3	CAP0G1	CAP0G6	CAP0B4	TCK	TMS	VSS	MA4	MA9	MA12		AB
AC		USART1_SCK	USART2_SOUT	USART3_SOUT	USART5_SIN	PWM_O6	SD0CMD	ISD0WP	I2S0_SDI	DISP1VI_1	DISP1VI_6	AD_VRL0	AD_VR1	CAP3VI_3	CAP2VI_1	CAP2VI_5	CAP1VI_2	CAP0R1	CAP0R5	CAP0G2	CAP0G7	CAP0B5	CAP0VAL	TDO	DDRVDE	MA3	MA8		AC
AD		USART2_SCK	USART3_SCK	PWM_O7	USART5_SOUT	OSDCLK0	ISD0CD	I2S1_ECLK	I2S0_ECLK	DISP1VI_2	DISP1VI_7	AD_VIN0	AD_VRH1	CAP3VI_4	CAP2VI_0	CAP2VI_4	CAP1VI_1	CAP1VI_5	CAP0R2	CAP0R7	CAP0G3	CAP0B0	CAP0B3	CAP0HS	TDI	MA0	MA2		AD
AE		VSS	USART4_SIN	VSS	PWM_O8	SD0DAT3	I2S1_SDO	I2S0_SDO	DISP1VI_0	DISP1VI_5	AD_VR0	AD_VIN1	CAP3VI_0	CAP3VI_5	CAP3VI_7	CAP2VI_3	CAP2VI_7	CAP1VI_3	CAP1VI_7	CAP0R4	CAP0G0	CAP0G4	CAP0B1	CAP0B6	CAP0B7	XSRST	MA1		AE
AF		VSS	VSS	USART4_SOUT	SD0DAT2	I2S1_WS	I2S1_SCK	I2S0_WS	DISP1VI_3	DISP1CLK	AD_AVD	AD_AVS	CAP3CLK	CAP3VI_1	CAP3VI_6	CAP2CLK	CAP2VI_6	CAP1CLK	VSS	CAP1VI_6	CAP0R6	CAP0CLK	CAP0G5	CAP0B2	CAP0VS	CAP0FID	VSS		AF
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26		

Figure 1.8. : MB86R11F pin assignment (pin name)

1.8.2.2. MB86R12/13 Pin Assignment



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	VSS	VSS	MEM_ED4	MEM_ED0	SPI0_SS	SPI0_SCK	MLB_SIG	I2C0_SDA	I2C0_SCL	VSS	VDDA	SDCLKT0M	SDCLKT1M	SDCLKT2M	VDDA	SDINRM	VCM0	VSSA	XTAL_XO	SELFL	CLKX0	VSS	VINTH	CRPM2	VSS	VSS	A
B	VSS	MEM_ED12	MEM_ED9	MEM_ED6	MEM_ED1	CAN0_TX	CAN0_RX	MLB_DATA	I2C1_SDA	INT_A5	VSSA	SDCLKT0P	SDCLKT1P	SDCLKT2P	VSSA	SDINRP	VDDA	VSSA	VDDEA	PLLBYPASS	INT_A2	VDDE	CRPM8	CRPM1	JTAG_TRST	VSS	B
C	MEM_ED2	MEM_XCS1	MEM_ED14	MEM_ED11	MEM_ED7	MEM_ED2	CAN1_TX	SPI0_DO	I2C1_SCL	INT_A6	VSSA	VDDA	VSSA	VDDA	VCMI	VSSA	ATST	XTAL_XI	VSSA	INT_A1	CLKX1	VSS	CRPM0	PSMODE	MPXMODE0	MD25	C
D	MEM_ED4	VSS	MEM_EA1	MEM_XCS0	MEM_ED13	MEM_ED8	MEM_ED3	CAN1_RX	MLB_CLK	INT_A7	VSSA	SDINT0M	SDINT1M	SDINT2M	VSSA	SDCLKTRM	VDDA	VSSA	SSCGVSS	SSCGVDD	VSS	XRST	MPXMODE2	TESTMODE	MD24	VSS	D
E	MEM_ED8	MEM_EA6	MEM_EA5	MEM_EA3	MEM_XCS2	MEM_ED15	MEM_ED5	MEM_ED10	SPI0_DI	INT_A4	VSSA	SDINT0P	SDINT1P	SDINT2P	VSSA	SDCLKTRP	VSSA	INT_A0	SSCGVSS	SSCGVDD	VPD	MPXMODE1	VSS	MD27	DDRVDE	VSS	E
F	MEM_EA12	MEM_EA11	MEM_EA10	MEM_EA9	MEM_EA7	VSS	VDDE	VDDE	VSS	VDDE	VSS	VDDA	VSSA	VDDA	VDDA_VCO	VSSA	VDDIA	VSS	VDD	VDDE	VSS	MAREF1	MD26	MDM8	MD03	MDQS3	F
G	MEM_EA16	VSS	MEM_EA15	MEM_EA14	MEM_EA13	VDDE															DDRVDE	MD28	MD30	MD23	MD29	VSS	G
H	MEM_EA17	MEM_EA18	MEM_EA19	MEM_EA22	MEM_EA20	MEM_EA21															DDRVDE	MD31	MD22	DDRVDE	MDQS2	MD02	H
J	MEM_EA23	MEM_EA24	MEM_EA25	MEM_EA26	MEM_XRD	MEM_XWR0															VSS	MD21	MD20	MD19	VSS	MDQ17	J
K	MEM_RDY	VSS	MEM_ALE	MEM_CLK	MEM_XWR1	VDD				VSS	VDD	VSS	VDD	VDD	VSS	VDD	VSS				VDD	MDM2	MDQ18	MDQ16	DDRVDE	VSS	K
L	MEM_CLE	MEM_MWREX	MEM_MWEX	MEM_XWR3	MEM_ED18	VSS				VDD	VSS	VSS	VSS	VSS	VSS	VSS	DDRVDE				VDD	MRCRES	MAREF2	VSS	MCK	MCK	L
M	MEM_XWR2	MEM_ED16	MEM_ED19	MEM_ED21	MEM_ED24	VDDE				VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS				VSS	MD28	MD09	MDQ10	DDRVDE	VSS	M
N	MEM_ED17	MEM_ED20	MEM_ED23	MEM_ED26	MEM_ED29	MEM_ED31				VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD				DDRVDE	MDQ11	MDM1	DDRVDE	MDQS1	MDQS1	N
P	MEM_ED22	MEM_ED25	MEM_ED27	MEM_ED28	MEM_ED30	VSS				VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD				DDRVDE	MDQ14	MDQ13	MDQ12	MDQ15	VSS	P
R	DISPOG3	DISPOG2	DISPOG1	DISPOG0	VDDE	VSS				VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS				VSS	MD05	MD06	MD04	VSS	MD07	R
T	DISPOR1	DISPOR0	DISPOG7	DISPOG6	DISPOG5	DISPOG4				VDD	VSS	VSS	VSS	VSS	VSS	VSS	DDRVDE				VDD	MAREF0	MDM0	DDRVDE	MDQS0	MDQ00	T
U	DISPOR7	DISPOR6	DISPOR5	DISPOR4	DISPOR3	DISPOR2				VSS	VDD	VSS	VDD	VDD	VSS	VDD	VSS				VDD	MD00	MD01	MD02	MD08	VSS	U
V	VSS	DISPOB3	DISPOB2	DISPOB1	DISPOB0	VDD															VSS	MDVE	MARAS	DDRVDE	MDDT	MARESET	V
W	DISPOB7	DISPOB6	DISPOB5	DISPOB4	DISPOHSYNC	DISPOCSYNC															DDRVDE	MA13	VSS	MCS	MCAS	MAVE	W
Y	DISPOCLKO	DISPOCLKCK	DISPOVSYNC	DISPODE	USART0_SIN	VDDE															DDRVDE	MA7	MA11	MA14	MBA1	MBA2	Y
AA	VSS	DISPOGV	USART0_SOUT	USART1_SOUT	USART2_SIN	VSS	VDDE	SDDDAT1	VDD	VSS	AD_AVD	AD_AVS	VDDE	VSS	VDD	CAP0R0	VDD	VSS	VDDE	XTRST	VSS	MA5	MA6	MA10	VSS	MBA0	AA
AB	DISPOCLKI	USART0_SCK	USART1_SIN	USART3_SIN	USART4_SCK	USART5_SCK	SDDDAT0	I2S1_SDI	I2S0_SCK	DISP1VI_4	AD_VRH0	AD_VRL1	CAP3VI_2	CAP2VI_2	CAP1VI_0	CAP1VI_4	CAP0R3	CAP0G1	CAP0G6	CAP0B4	TCK	TMS	VSS	MA4	MA9	MA12	AB
AC	USART1_SCK	USART2_SOUT	USART3_SOUT	USART5_SIN	PWMO6	SDDCMD	I SDDWP	I2S0_SDI	DISP1VI_1	DISP1VI_6	AD_VRL0	AD_VR1	CAP3VI_3	CAP2VI_1	CAP2VI_5	CAP1VI_2	CAP0R1	CAP0R5	CAP0G2	CAP0G7	CAP0B5	CAP0VAL	TDO	DDRVDE	MA3	MA8	AC
AD	USART2_SCK	USART3_SCK	PWMO7	USART5_SOUT	SDDCLKO	I SDDCD	I2S1_ECLK	I2S0_ECLK	DISP1VI_2	DISP1VI_7	AD_VINO	AD_VRH1	CAP3VI_4	CAP2VI_0	CAP2VI_4	CAP1VI_1	CAP1VI_5	CAP0R2	CAP0R7	CAP0G3	CAP0B0	CAP0B3	CAP0HS	TDI	MA0	MA2	AD
AE	VSS	USART4_SIN	VSS	PWMO8	SDDDAT3	I2S1_SDO	I2S0_SDO	DISP1VI_0	DISP1VI_5	AD_VR0	AD_VINI	CAP3VI_0	CAP3VI_5	CAP3VI_7	CAP2VI_3	CAP2VI_7	CAP1VI_3	CAP1VI_7	CAP0R4	CAP0G0	CAP0G4	CAP0B1	CAP0B6	CAP0B7	RSRST	MA1	AE
AF	VSS	VSS	USART4_SOUT	SDDDAT2	I2S1_VIS	I2S1_SCK	I2S0_VIS	DISP1VI_3	DISP1CLK	AD_AVD	AD_AVS	CAP3CLK	CAP3VI_1	CAP3VI_6	CAP2CLK	CAP2VI_6	CAP1CLK	VSS	CAP1VI_6	CAP0R6	CAP0CLK	CAP0G5	CAP0B2	CAP0VS	CAP0FID	VSS	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 1.9. : MB86R12/13 pin assignment (pin name)

1.8.3. Pin Descriptions

Refer to the attached files for the functional description of each pin and the functional groups.

MB86R11-PinList.xls

MB86R12_Pinlist.xlsx

MB86R13_Pinlist.xlsx

2. Electric Characteristics

2.1. Maximum Ratings

Table 2.1 and Table 2.2 , and Table 2.3 show the maximum ratings.

Table 2.1. : Maximum rating

Parameter	Symbol	Rating		Unit
Supply voltage	VDD SSCG0VDD SSCG1VDD VDDE DDRVDE	–0.5 to 1.8 [1)] –0.5 to 1.8 [2)] –0.5 to 1.8 [2)] –0.5 to 4.0 [3)] –0.5 to 2.5 [4)]		V
Input voltage	V_I	–0.5 to VDD + 0.5 (< 1.8V) –0.5 to VDDE + 0.5 (< 4.0V) –0.5 to DDRVDE + 0.5 (< 2.5V)		V
Output voltage	V_O	–0.5 to VDD + 0.5 (< 1.8V) –0.5 to VDDE + 0.5 (< 4.0V) –0.5 to DDRVDE + 0.5 (< 2.5V)		V
Storage temperature	T_{ST}	–55 to 125		°C
Junction temperature	T_J	–40 to 125		°C
Supply current	I_D	MB86R11F VDD: 3000 VDDE: 100 DDRVDE (1.5V, 800Mbps): 350 DDRVDE (1.8V, 800Mbps): 400	MB86R12/13 VDD: 3330[5)] VDDE: 100[5)] DDRVDE (1.5V, 1066Mbps): 450[5)] DDRVDE (1.8V, 800Mbps): 400[5)]	mA

1): Internal power supply
2): Power supply for PLL
3): Power supply for I/O
4): Power supply for SSTL_15 I/O
5): Current specification necessary for each voltage power supply,0

Note:

- Applying stress exceeding the maximum ratings (voltage, current, temperature, etc.) may cause damage to semiconductor devices. Never exceed the ratings above.
- Never connect IC outputs or I/O pins directly, or connect them to V_{DD} or V_{SS} directly; otherwise thermal destruction of elements will result, but which does not apply to pins designed to prevent signal collision.
- Provide ESD protection, such as grounding when handling the product; otherwise externally charged electric charge flows inside the IC and discharges, which may result in damage to the circuit.
- Applying voltage higher than V_{DD} or lower than V_{SS} to I/O pins of CMOS IC, or applying voltage higher than the ratings between V_{DD} and V_{SS} may cause latch up. The latch up increases supply current, resulting in thermal destruction of elements. Never exceed the maximum ratings.

Table 2.2. : ADC maximum rating

Parameter	Symbol	Rating	Unit
Supply voltage	AD_AVD	−0.5 to 4.0	V
Input voltage	AD_VRH0 AD_VRH1 AD_VRL0 AD_VRL1 AD_VIN0 AD_VIN1	−0.5 to VDDE + 0.5 (< 4.0V)	V
Output voltage	AD_VR0 AD_VR1	−0.5 to VDDE + 0.5 (< 4.0V)	V
Junction temperature	T_J	−40 to 125	°C

Table 2.3. : USB maximum ratings

Parameter	Symbol	Rating	Unit
Supply voltage	USBx_AVDF1 USBx_AVDB	Vss-0.5 to 4.0	V
	USBx_AVDF2 USBx_AVDP	Vss-0.5 to 1.8	V
Junction temperature	T_J	-40 to 125	°C
Supply current	USBx_AVDF1 USBx_AVDB	Total 37.5	mA
	USBx_AVDF2	19.2	mA
	USBx_AVDP	13.0	mA

The maximum ratings are the limits that must not be exceeded. As long as USB PHY is used withing the range predetermined in the maximum ratings, it will not summer permanent damage. However, this does not ensure normal logic operation.

Table 2.4. : Thermal design

Device	Package	Φ_{JA*}	Ψ_{JT**}	Operating temperature in °C	
		in K/W		Ta	Tc
MB86R11F	PBGA	16.3	1.0	–40 to 85	–40 to 105
MB86R12 / MB86R13	TEBGA	13	2.5	–40 to 85	–40 to 105

Φ_{JA}Junction-to-ambient thermal resistance
Ψ_{JT}Junction-to-top characterization parameter
TaAmbient temperature
TcCase temperature
TjJunction temperature
*Measured according to JEDEC standard (with standard board 100x100mm, standard test environment)
** Measured with test chip on 84x117mm 4-layer board.

Important: Both temperature conditions must be satisfied!

Note:

- To ensure that the MB86R11F/12/13 device does not exceed the maximum T_c during operation, an adequate thermal solution must be designed
- If the MB86R11F/12/13 exceeds the maximum T_C during operation, the device functionality is not guaranteed.

2.2. Recommended Operating Conditions

Table 2.5 shows 3.3V standard CMOS I/O recommended operating conditions

Table 2.5. : 3.3V standard CMOS I/O recommended operating conditions

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply voltage		VDDE	3.0	3.3	3.6	V
		VDD SSCG0VDD SSCG1VDD	1.1	1.2	1.3	V
		VDDEA VDDA VDDA_VCO VDDIA	3.0 1.1 1.1 1.1	3.3 1.2 1.2 1.2	3.6 1.3 1.3 1.3	V
Input voltage (High level)	3.3V CMOS	VIH	2.0	-	VDDE + 0.3	V
	3.3V CMOS Schmitt		2.1	-	VDDE + 0.3	V
Input voltage (Low level)	3.3V CMOS	VIL	–0.3	-	0.8	V
	3.3V CMOS Schmitt		–0.3	-	0.7	V
Schmitt hysteresis voltage		V_H	0.2	-	1.4	V

Table 2.6. : SSTL15 IO(SSTL15 mode) recommended operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage	DDRVDE	1.425	1.500	1.575	V
	VDD	1.10	1.20	1.30	V
Reference voltage	V_{REF}	DDRVDEx0.49	DDRVDEx0.5	DDRVDEx0.51	V
Termination voltage	V_{TT}	-	DDRVDE/2	-	V
H level input Single (DC)	$V_{IH(DC)}$	V_{REF} + 0.1	-	DDRVDE	V
L level input Single (DC)	$V_{IL(DC)}$	VSS	-	V_{REF} – 0.1	V
H level input Single (AC)	$V_{IH(AC)}$	V_{REF} + 0.175	-	*)	V
L level input Single (AC)	$V_{IL(AC)}$	*)	-	V_{REF} – 0.175	V
H level input Differential (DC)	$V_{IHdiff(DC)}$	0.2	-	*)	V
L level input Differential (DC)	$V_{ILdiff(DC)}$	*)	-	–0.2	V
H level input Differential (AC)	$V_{IHdiff(AC)}$	0.35	-	*)	V
L level input Differential (AC)	$V_{ILdiff(AC)}$	*)	-	–0.35	V
Standard SSTL15 recommended operating conditions (except from JESD79-3E) *): Overshoot / Undershoot rule of JESD79-3E.					

Table 2.7. : SSTL15 IO(SSTL18 mode) recommended operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage	DDRVDE	1.7	1.8	1.9	V
	VDD	1.10	1.20	1.30	V
Reference voltage	V_{REF}	DDRVDEx0.49	DDRVDEx0.5	DDRVDEx0.51	V
Termination voltage	V_{TT}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
H level input Single (DC)	$V_{IH(DC)}$	V_{REF} + 0.125	-	DDRVDE + 0.3	V
L level input Single (DC)	$V_{IL(DC)}$	–0.3	-	V_{REF} – 0.125	V
H level input Single (AC)	$V_{IH(AC)}$	V_{REF} + 0.200	-	VDE + 0.3	V
L level input Single (AC)	$V_{IL(AC)}$	–0.3	-	V_{REF} – 0.200	V
Standard SSTL15(SSTL18 mode) recommended operating conditions (except from JESD79-2E)					

Table 2.8. : USB recommended operation condition

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply voltage	USBx_AVDF1 USBx_AVDB	3.0	3.3	3.6	V
	USBx_AVDF2	1.1	1.2	1.3	V
	USBx_AVDP	1.1	1.2	1.3	V
The clock input to USBx_CRYCLK48 should be meet the following requirements. - Clock of 48MHz±110ppm - Jetta of 100ps or less					

Note:

- The recommended operating conditions are primarily intended to assure the normal operation of semiconductor device.
- The values of electrical characteristics are guaranteed under the requirements above, so use the product accordingly.
- Using the product without observing the conditions may affect the product's reliability.
- Performance of this product is not guaranteed if used under unspecified conditions and by an unspecified combination of logic.
- Supply power ON/OFF so that power for SSCG0VDD/SSCG1VDD does not exceed VDD.
- All powers must be supplied.

2.3. Power ON

2.3.1. Recommended Power ON/OFF Sequence

The recommended order of power supply turning On/Off is as follows:

Power On: VDD, SSCG0VDD, SSCG1VDD → DDRVDE → VDDE → generic signal

Power Off: Generic signal → VDDE → DDRVDE → VDD, SSCG0VDD, SSCG1VDD

Note: After VDD is switched On, there is no time limit to switch On/Off other power supplies.

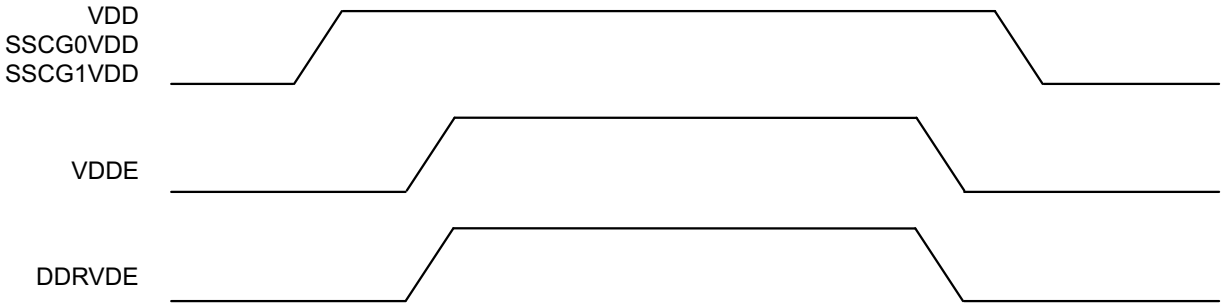
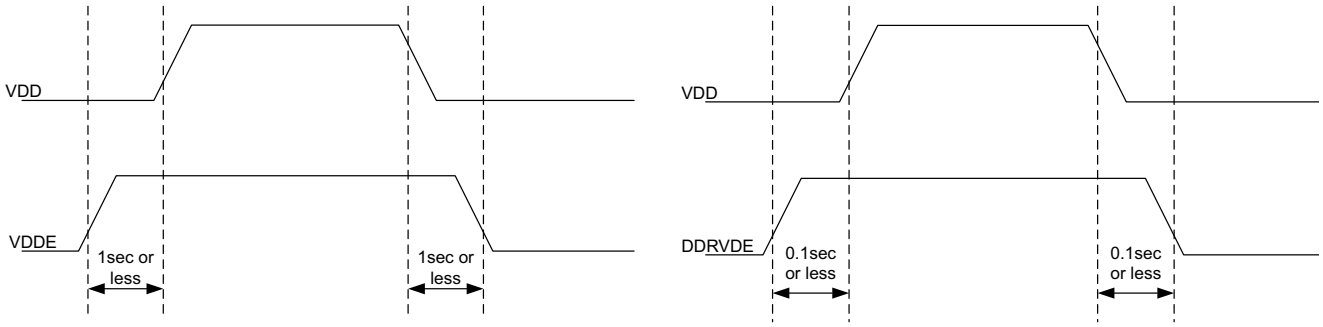


Figure 2.1. : The order of recommended power supply

2.3.2. Alternative Power ON/OFF Sequence (not recommended)

When VDDE and/or DDRVDE power supply are turned On before VDD, the following limitations must be considered. See Figure 2.2.



Note:
- Do not continuously supply VDDE longer than 1sec, if VDD is not supplied.
- Do not continuously supply DDRVDE longer than 0.1sec, if VDD is not supplied

Figure 2.2. : The order of alternative power supply (not recommended)

Note: As long as VDD is not supplied, bus conflict of external pins may occur due to undefined IO level and direction.

2.3.3. Power ON Timing Chart

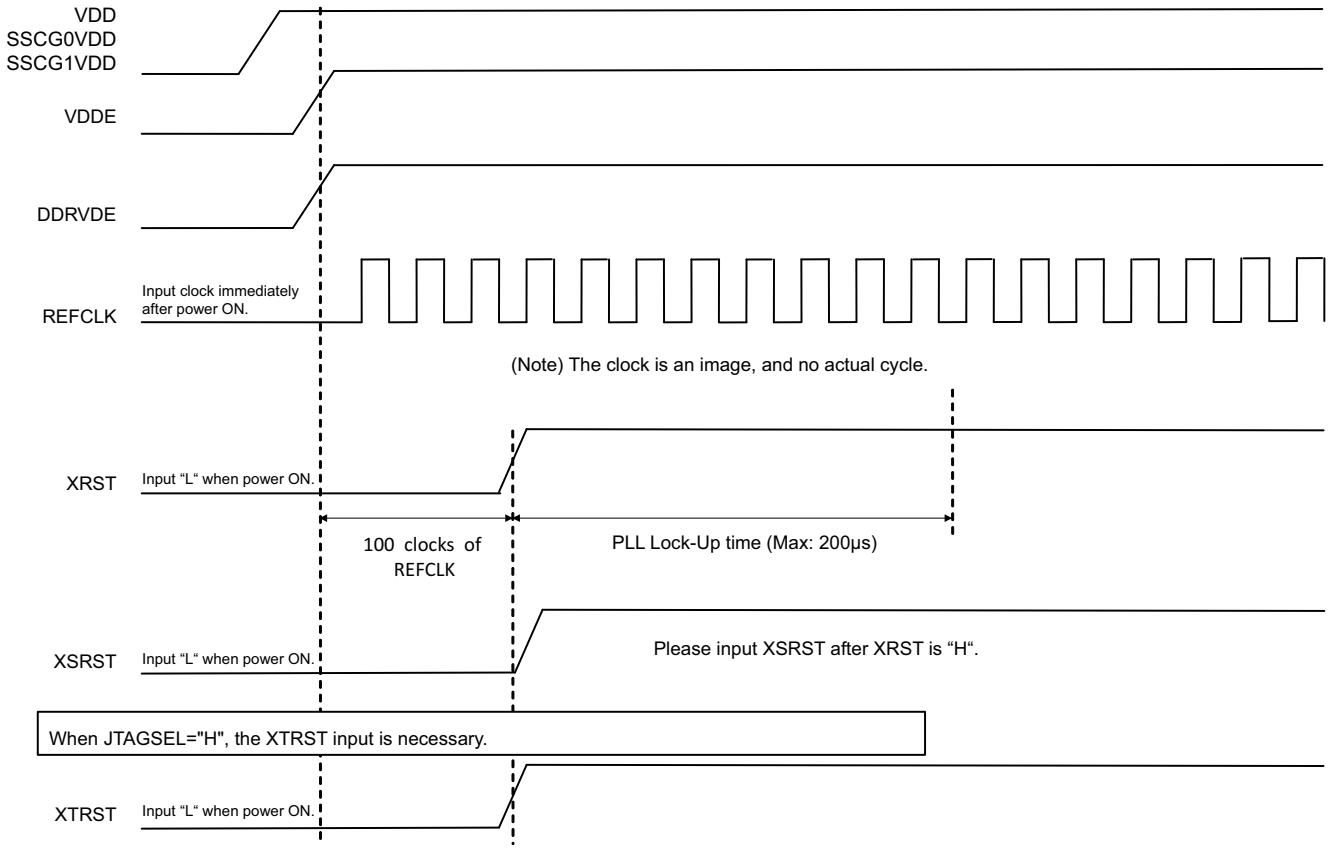


Figure 2.3. : Power on timing chart

Note:

- Input REFCLK immediately after power ON.
- Input the XTRST, XRST pins to 'Low' when power ON.
- Keep the XTRST and XRST pins 'High' after input "L" for at least 100 clocks of REFCLK. For example: 25MHz needs 4µs, 33.33MHz needs 3µs.
- After PLL LockUp Time, registers can be accessed.

2.3.4. Power On Inrush Current

When powering On the 1.2V supply (VDD), the inrush current drawn by the chip might be higher than the maximum current under full work load of the chip.

The relevant max values are shown in Table 2.9 . Please dimension the power supply accordingly or increase the slew rate.

The inrush current has no influence to life-time of the device.

Refer to the table below.

Table 2.9. : Power ON inrush current

Supply slew rate	1ms	3ms	5ms	10ms	50ms	100ms
VDDI inrush current (Max.[1])	7.420A	4.11A	2.444A	1.438A	0.413A	0.243A
VDDI inrush current (Typ.)	0.622A	0.45A	0.126A	0.066A	0.015A	0.008A

[1] Max condition: Tj = -40 °C , VDD = 1.3V

2.4. DC Characteristics

2.4.1. 3.3V Standard CMOS I/O

Table 2.10 shows 3.3V Standard CMOS I/O DC characteristics.

Measurement condition: VDDE = 3.3 ±0.3 V, VSS = 0 V, T_j = –40 to 125°C

Table 2.10. : Standard CMOS I/O DC characteristics

Parameter	Symbol	Condition		Rating			Unit
				Min	Typ	Max	
H level input voltage	V_{IH}			2.0	-	VDDE + 0.3	V
L level input voltage	V_{IL}			–0.3	-	0.8	V
H level output voltage	V_{OH}	IOH = –100mA		VDDE – 0.2	-	VDDE	V
L level output voltage	V_{OL}	IOL = 100mA		0	-	0.2	V
H level output V-I characteristic	-	Driving capability 2mA	I_{OH} = 2mA	Refer to Figure 2.4, Figure 2.5, and Figure 2.6			-
		Driving capability 4mA	I_{OH} = 4mA				
		Driving capability 6mA	I_{OH} = 6mA				
		Driving capability 8mA	I_{OH} = 8mA				
L level output V-I characteristic	-	Driving capability 2mA	I_{OH} = 2mA				-
		Driving capability 4mA	I_{OH} = 4mA				
		Driving capability 6mA	I_{OH} = 6mA				
		Driving capability 8mA	I_{OH} = 8mA				
Input leakage current	I_L			-	-	±10	µA
Pull-up/pull-down resistance	R_p	Pull-up V_{IL}=0V Pull-down V_{IH}= VDDE		15	33	70	kΩ

2.4.1.1. 3.3V Standard CMOS I/O V-I Characteristic (Driving Capability 2mA)

Conditions:

MIN: Process = Slow T_J = 125°C VDDE = 3.0 V

TYP: Process = Typical T_J = 25°C VDDE = 3.3 V

MAX: Process = Fast T_J = –40°C VDDE = 3.6 V

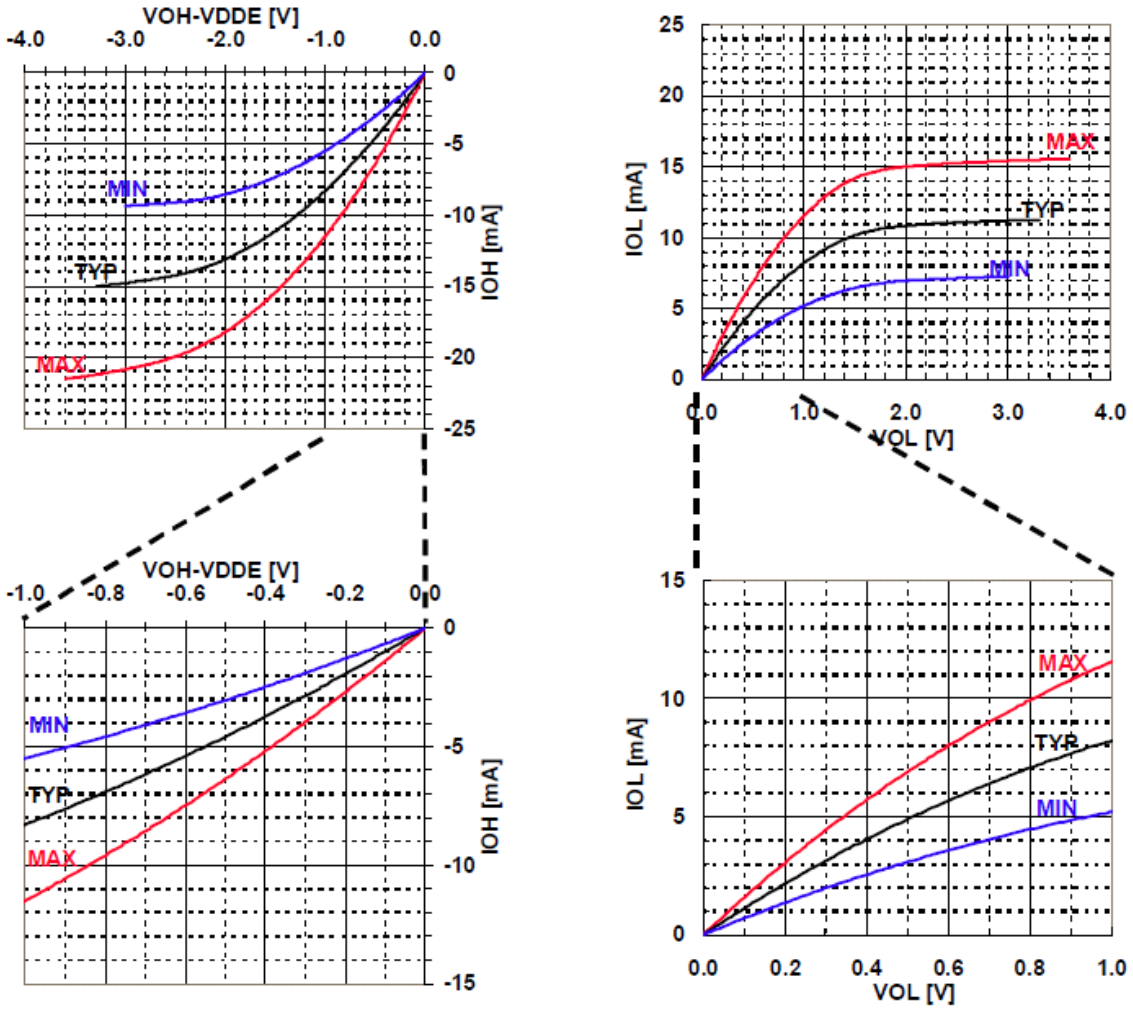


Figure 2.4. : 3.3V standard CMOS I/O V-I characteristic (Driving capability 2mA)

2.4.1.2. 3.3V Standard CMOS I/O V-I Characteristic (Driving Capability 4mA)

Conditions

MIN: Process = Slow T_J = 125°C VDDE = 3.0 V

TYP: Process = Typical T_J = 25°C VDDE = 3.3 V

MAX: Process = Fast T_J = –40°C VDDE = 3.6 V

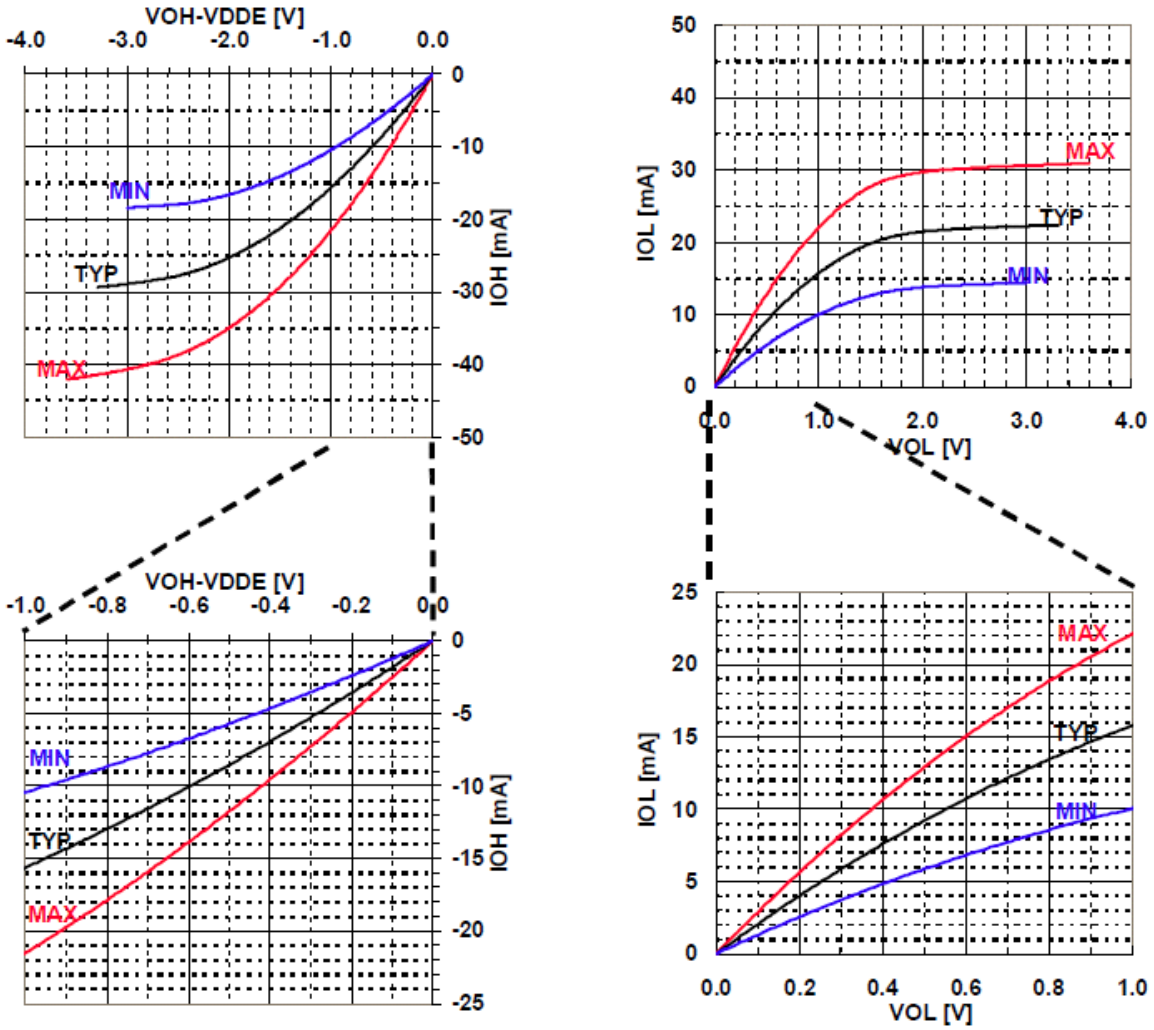


Figure 2.5. : 3.3V standard CMOS I/O V-I characteristic (Driving capability 4mA)

2.4.1.3. 3.3V Standard CMOS I/O V-I Characteristic (Driving capability 6mA)

Conditions

MIN: Process = Slow T_J = 125°C VDDE = 3.0 V

TYP: Process = Typical T_J = 25°C VDDE = 3.3 V

MAX: Process = Fast T_J = –40°C VDDE = 3.6 V

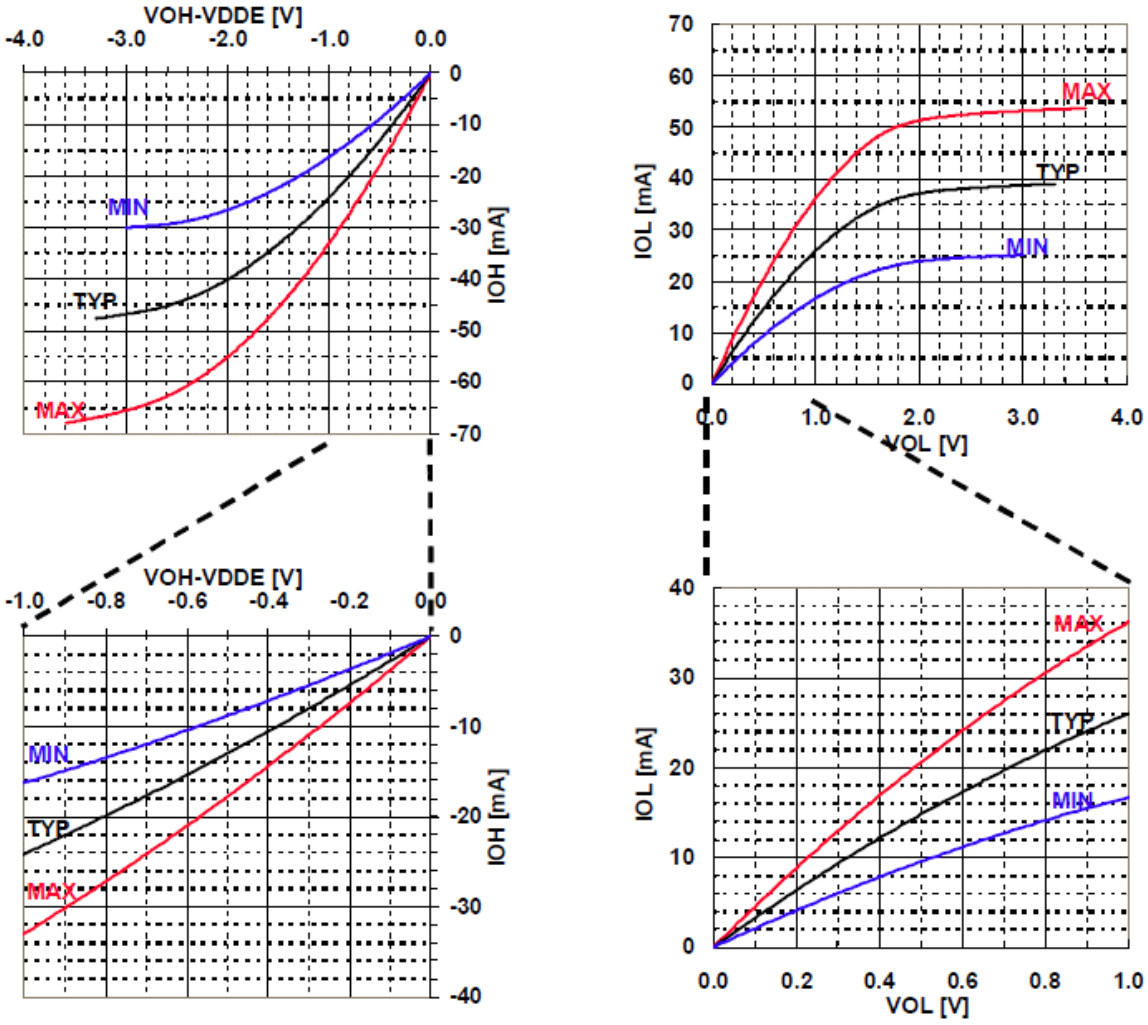


Figure 2.6. : 3.3V standard CMOS I/O V-I characteristic (Driving capability 6mA)

2.4.1.4. 3.3V Standard CMOS I/O V-I Characteristic (Driving capability 8mA)

Conditions

MIN: Process = Slow T_J = 125°C VDDE = 3.0 V

TYP: Process = Typical T_J = 25°C VDDE = 3.3 V

MAX: Process = Fast T_J = –40°C VDDE = 3.6 V

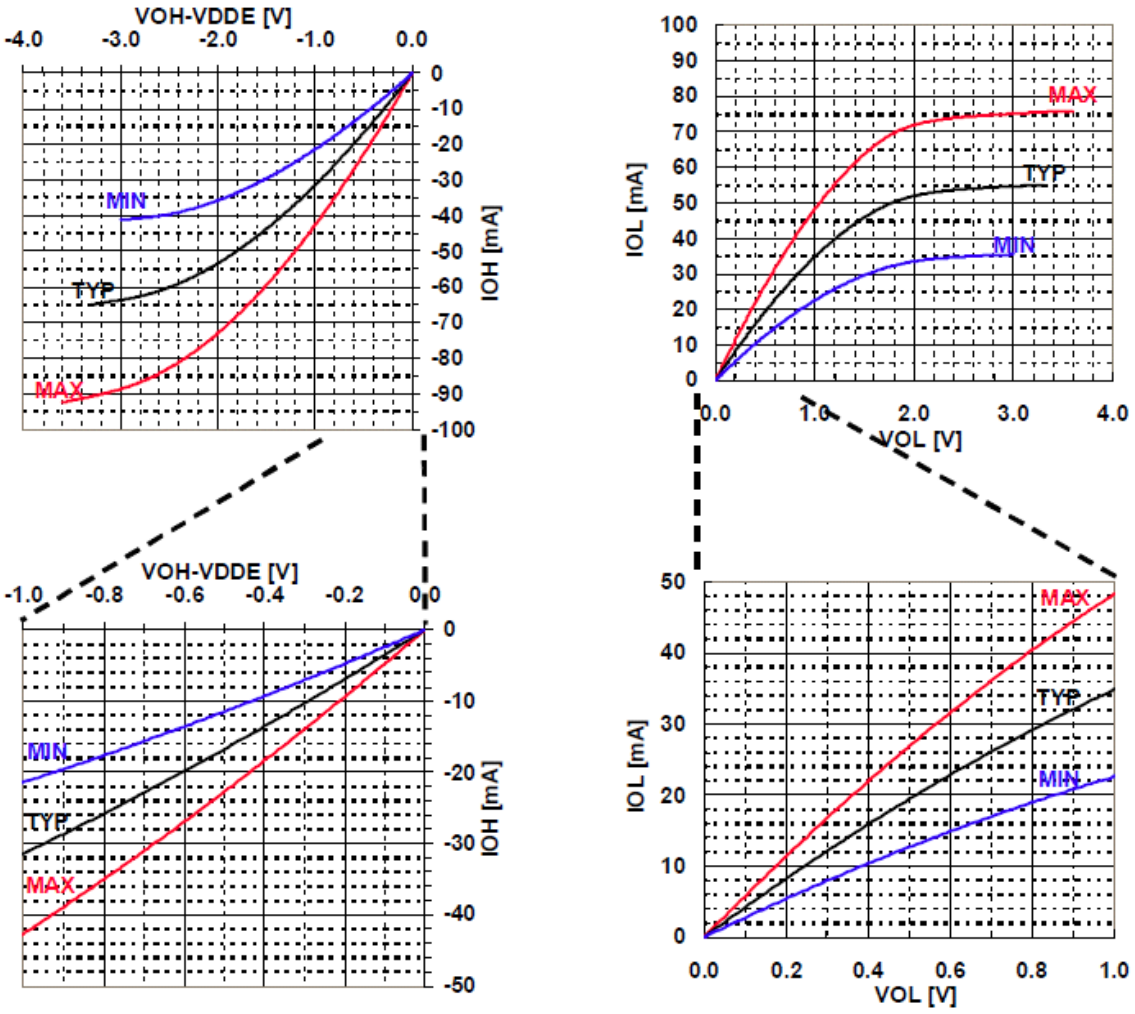


Figure 2.7. : 3.3V standard CMOS I/O V-I characteristic (Driving capability 8mA)

2.4.2. SSTL15 I/O

Table 2.11. : Output Driver DC Characteristics, assuming RZQ=240Ω by SSTL15 mode

RONnom	Resistor	Vout	Min	Nom	Max	Unit	Notes
34	RON34pd	V_{OLdc}=0.2xDDRVDE	0.6	1.0	1.1	RZQ/7	1)
		V_{OMdc}=0.5xDDRVDE	0.9	1.0	1.1	RZQ/7	1)
		V_{OHdc}=0.8xDDRVDE	0.9	1.0	1.4	RZQ/7	1)
	RON34pu	V_{OLdc}=0.2xDDRVDE	0.9	1.0	1.4	RZQ/7	1)
		V_{OMdc}=0.5xDDRVDE	0.9	1.0	1.1	RZQ/7	1)
		V_{OHdc}=0.8xDDRVDE	0.6	1.0	1.1	RZQ/7	1)
40	RON40pd	V_{OLdc}=0.2xDDRVDE	0.6	1.0	1.1	RZQ/6	1)
		V_{OMdc}=0.5xDDRVDE	0.9	1.0	1.1	RZQ/6	1)
		V_{OHdc}=0.8xDDRVDE	0.9	1.0	1.4	RZQ/6	1)
	RON40pu	V_{OLdc}=0.2xDDRVDE	0.9	1.0	1.4	RZQ/6	1)
		V_{OMdc}=0.5xDDRVDE	0.9	1.0	1.1	RZQ/6	1)
		V_{OHdc}=0.8xDDRVDE	0.6	1.0	1.1	RZQ/6	1)
48	RON48pd	V_{OLdc}=0.2xDDRVDE	0.6	1.0	1.1	RZQ/5	1)
		V_{OMdc}=0.5xDDRVDE	0.9	1.0	1.1	RZQ/5	1)
		V_{OHdc}=0.8xDDRVDE	0.9	1.0	1.4	RZQ/5	1)
	RON48pu	V_{OLdc}=0.2xDDRVDE	0.9	1.0	1.4	RZQ/5	1)
		V_{OMdc}=0.5xDDRVDE	0.9	1.0	1.1	RZQ/5	1)
		V_{OHdc}=0.8xDDRVDE	0.6	1.0	1.1	RZQ/5	1)
60	RON60pd	V_{OLdc}=0.2xDDRVDE	0.6	1.0	1.1	RZQ/4	1)
		V_{OMdc}=0.5xDDRVDE	0.9	1.0	1.1	RZQ/4	1)
		V_{OHdc}=0.8xDDRVDE	0.9	1.0	1.4	RZQ/4	1)
	RON60pu	V_{OLdc}=0.2xDDRVDE	0.9	1.0	1.4	RZQ/4	1)
		V_{OMdc}=0.5xDDRVDE	0.9	1.0	1.1	RZQ/4	1)
		V_{OHdc}=0.8xDDRVDE	0.6	1.0	1.1	RZQ/4	1)
Mismatch between pull-up and pull-down, MM_{PuPd}		V_{OMdc} 0.5xDDRVDE	−10	-	+10	%	1), 2)

1): The tolerance limits are specified after calibration with stable voltage and temperature.
2): Mismatch specification between pull-up and pull-down output impedances. Both the RONpu and RONpd are defined by 0.5 x DDRVDE. (See the equation below.)

$$MM_{PuPd} = \frac{RON_{Pu} - RON_{Pd}}{RON_{Nom}} \times 100$$

Table 2.12. : Output Driver DC Characteristics, assuming RZQ=200Ω by SSTL18 mode

RONnom	Resistor	Vout	Min	Nom	Max	Unit	Notes
28.6	RON28pd	V_{OMdc}=0.5xDDRVDE	0.85	1.0	1.15	RZQ/7	1), 2)
	RON28pu	V_{OMdc}=0.5xDDRVDE	0.85	1.0	1.15	RZQ/7	1), 2)
33.3	RON33pd	V_{OMdc}=0.5xDDRVDE	0.85	1.0	1.15	RZQ/6	1), 2)
	RON33pu	V_{OMdc}=0.5xDDRVDE	0.85	1.0	1.15	RZQ/6	1), 2)
40	RON40pd	V_{OMdc}=0.5xDDRVDE	0.85	1.0	1.15	RZQ/5	1), 2)
	RON40pu	V_{OMdc}=0.5xDDRVDE	0.85	1.0	1.15	RZQ/5	1), 2)
50	RON50pd	V_{OMdc}=0.5xDDRVDE	0.85	1.0	1.15	RZQ/4	1)
	RON50pu	V_{OMdc}=0.5xDDRVDE	0.85	1.0	1.15	RZQ/4	1)
Mismatch between pull-up and pull-down, MM_{PuPd}		V_{OMdc} 0.5xDDRVDE	-15	-	+15	%	1), 2)

1): The tolerance limits are specified after calibration with stable voltage and temperature.

2): Mismatch specification between pull-up and pull-down output impedances. Both the RONpu and RONpd are defined by 0.5 x DDRVDE. (See the equation below.)

$$MM_{PuPd} = \frac{RON_{Pu} - RON_{Pd}}{RON_{Nom}} \times 100$$

$$RON_{Pu} = \frac{DDRVDE - V_{Out}}{|I_{Out}|}$$

under the condition that RON_{Pd} is turned Off

$$RON_{Pd} = \frac{V_{Out}}{|I_{Out}|}$$

under the condition that RON_{Pu} is turned Off

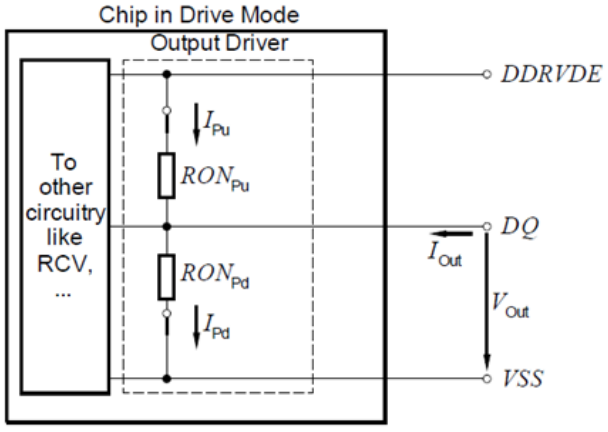


Figure 2.8. : Output driver DC characteristics definition

Table 2.13. : ODT DC Characteristics, assuming RZQ=240Ω by SSTL15 mode

RTT	Resistor	Vout	Min	Nom	Max	Unit	Notes
120	RTT120pd240	V_{OLdc}=0.2xDDRVDE	0.6	1.0	1.1	RZQ	1)
		0.5xDDRVDE	0.9	1.0	1.1	RZQ	1)
		V_{OHdc}=0.8xDDRVDE	0.9	1.0	1.4	RZQ	1)
	RTT120pu240	V_{OLdc}=0.2xDDRVDE	0.9	1.0	1.4	RZQ	1)
		0.5xDDRVDE	0.9	1.0	1.1	RZQ	1)
		V_{OHdc}=0.8xDDRVDE	0.6	1.0	1.1	RZQ	1)
	RTT120	$V_{IL(ac)}$ to VIH(ac)	0.9	1.0	1.6	RZQ/2	1), 2)
60	RTT60pd120	V_{OLdc}=0.2xDDRVDE	0.6	1.0	1.1	RZQ/2	1)
		0.5xDDRVDE	0.9	1.0	1.1	RZQ/2	1)
		V_{OHdc}=0.8xDDRVDE	0.9	1.0	1.4	RZQ/2	1)
	RTT60pu120	V_{OLdc}=0.2xDDRVDE	0.9	1.0	1.4	RZQ/2	1)
		0.5xDDRVDE	0.9	1.0	1.1	RZQ/2	1)
		V_{OHdc}=0.8xDDRVDE	0.6	1.0	1.1	RZQ/2	1)
	RTT60	$V_{IL(ac)}$ to VIH(ac)	0.9	1.0	1.6	RZQ/4	1)
40	RTT40pd80	V_{OLdc}=0.2xDDRVDE	0.6	1.0	1.1	RZQ/3	1)
		0.5xDDRVDE	0.9	1.0	1.1	RZQ/3	1)
		V_{OHdc}=0.8xDDRVDE	0.9	1.0	1.4	RZQ/3	1)
	RTT40pu80	V_{OLdc}=0.2xDDRVDE	0.9	1.0	1.4	RZQ/3	1)
		0.5xDDRVDE	0.9	1.0	1.1	RZQ/3	1)
		V_{OHdc}=0.8xDDRVDE	0.6	1.0	1.1	RZQ/3	1)
	RTT40	$V_{IL(ac)}$ to VIH(ac)	0.9	1.0	1.6	RZQ/6	1)
Deviation of VM w.r.t VDE/2, DVM			–7	-	+7	%	1), 3)

1) Defined as the specification after calibration under stable voltage and temperature.

2) Definition of RTT measurement.

$$RTT = \frac{V_{IH(ac)} - V_{IL(ac)}}{I(V_{IH(ac)}) - I(V_{IL(ac)})}$$

3) ΔVM definition. In the DRAM specification, it is specified as ±5%. However, for the SSTL15 I/O buffers, it is specified as ±7%. The values are calculated from the intermediate voltage (VM) when the ODT impedances of the test pins without load are balanced.

$$\Delta V_M = \left(\frac{2 \times V_M}{DDRVDE} - 1\right) \times 100$$

Table 2.14. : ODT DC Characteristics, assuming RZQ=200Ω by SSTL18 mode

RTT	Resistors	Yout	Min	Nom	Max	Unit	Notes
100	RTT100pd200	0.5xDDRVDE	0.85	1.0	1.15	RZQ	1)
	RTT100pu200	0.5xDDRVDE	0.85	1.0	1.15	RZQ	1)
	RTT100	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.80	1.0	1.2	RZQ/2	1),2)
50	RTT50pd100	0.5xDDRVDE	0.85	1.0	1.15	RZQ/2	1)
	RTT50pu100	0.5xDDRVDE	0.85	1.0	1.15	RZQ/2	1)
	RTT50	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.80	1.0	1.2	RZQ/4	1),2)
Deviation of VM w.r.t VDE/2, DVM			–6	-	+6	%	1),3)

1) Defined as the specification after calibration under stable voltage and temperature.
2) Definition of RTT measurement.

$$RTT = \frac{V_{IH(ac)} - V_{IL(ac)}}{I(V_{IH(ac)}) - I(V_{IL(ac)})}$$

3) ΔVM definition. In the DRAM specification, it is specified as ±6%. And, for the SSTL15 I/O buffers, it is specified as ±6%. The values are calculated from the intermediate voltage (VM) when the ODT impedances of the test pins without load are balanced.

$$\Delta V_M = \left(\frac{2 \times V_M}{DDRVDE} - 1\right) \times 100$$

$$RTT_{Pu} = \frac{DDRVDE - V_{Out}}{|I_{Out}|}$$

under the condition that RTT_{Pd} is turned Off

$$RTT_{Pd} = \frac{V_{Out}}{|I_{Out}|}$$

under the condition that RTT_{Pu} is turned Off

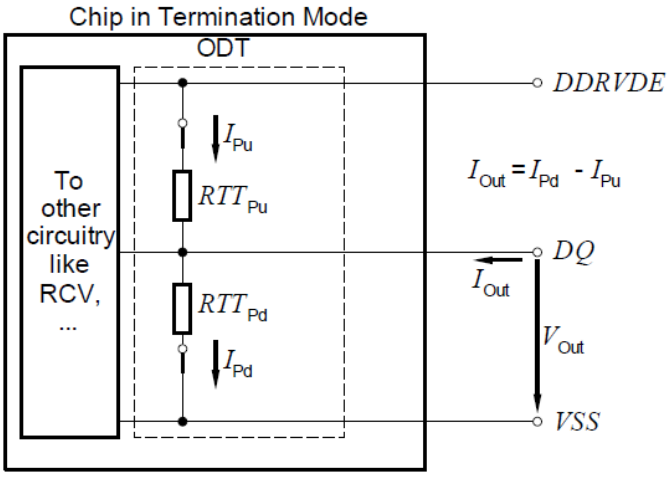


Figure 2.9. : ODT DC Characteristics Definition

2.4.3. ADC I/O

Table 2.15. : Recommended operating conditions

Parameter	Symbol	Pin Name	Specification			Units
			Min	Typ	Max	
Power Supply Voltage	V_{vd}	VDD	1.10	1.20	1.30	V
	V_{avd}	AD_AVD	2.70	3.00	3.60	V
Reference Voltage(H)	V_{rh}	AD_VRH0, AD_VRH1	V_{avd} – 0.05	-	V_{avd}	V
Reference Voltage(L)	V_{rl}	AD_VRL0, AD_VRL1	Vss 1)	-	Vss+0.05	V
Decoupling Capacitor	C_{ref} 2), 5)	AD_VR0, AD_VR1	0.1	-	-	uF
Analog Input Voltage	V_{in}	AD_VIN0, AD_VIN1	V_{rl}	-	V_{rh}	V
Analog Input Frequency	F_{vin}	AD_VIN0, AD_VIN1	0	-	Fs/2	Hz
Conversion Rate	Fs 3)	STC	-	-	500.0	KS/s
Clock Frequency	Fc 3)	CLK	8M 4)	-	10M	Hz
Number of Sampling Clock	Ns 3)	CLK	2	-	-	-
Number of Conversion Clock	Nc 3)	CLK	14	-	-	-
Junction Temperature	T_j	-	–40	-	125	°C

1) V_{SS} = AD_AVS (Analog GND)

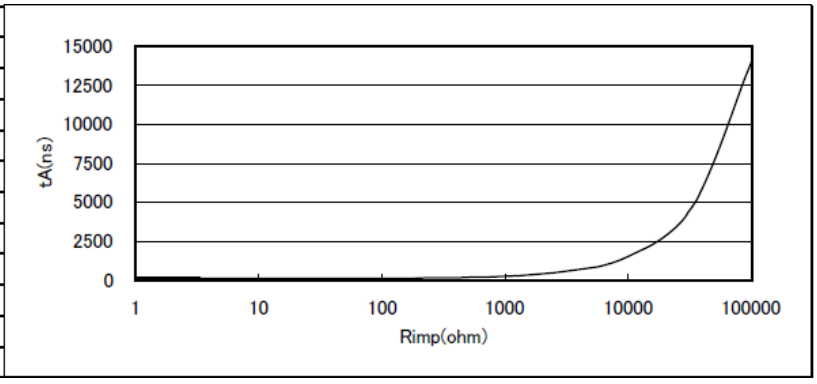
2) A/D outputs incorrect result at the instant following power on or at the resumption from power-down mode.

3) FC = FS x (NS+NC)
The conversion rate is dependent on output impedance drive the VIN.
Choose the FC or NS to satisfy the expression [Sampling time > t A]
There are two types of timing that sampling starts: soon after conversion ends and soon after up of STC.
Sampling ends soon after the first up of CLK after the down of STC.
Rimp is output impedance of the driver drives VIN.
To put the error of the sampled analog input in 0.5LSB or less, the relation between t A and Rimp is shown in the figure below.

4) Except for convert period, these signals can be specified DC signal.

5) Resumption Time has a relationship with the capacity value of external capacity.

Rimp[ohm]	tA[ns]
1	139
3.3	139
10	140
33	143
100	153
330	185
1000	278
3300	597
10000	1527
33000	4718
100000	14016



In case after the power down is released, follow resumption time.

Table 2.16. : ADC characteristic

Parameter	Symbol	Pin Name	Conditions	Specification			Units
				Min	Typ	Max	
Resolution	BIT	-		-	-	12	Bits
Supply Current	I_{VD}	VDD		-	-	0.1	mA
	I_{AVD}	AD_AVD	$V_{RH}=A_{VDH}$ $V_{RL}=A_{VS}$		1.0	1.6	mA
	I_{DS}	VDD,AD_AVD	XPD="0"	0	-	60	uA
Input Leak Current	I_{VINon}	AD_VIN0, AD_VIN1	Selected VIN	−1.2	-	0.6	uA
Reference Voltage(M)	V_R	AD_VR0, AD_VR1	V_{IN}="V_{avd}/2"	−2.0	$(V_{rh}+V_{rl})/2$	2.0	V%
Reference Resistance	R_R	AD_VRH0, AD_VRH1, AD_VRL0, AD_VRL1	Between V_{RH} and V_{RL}	4.1	6.6	10.2	Kohm
Zero Transition Voltage 6)	V_{ZT}	-	Between 0 and 1	Typ-20	$V_{rl}+(V_{rh}-V_{rl})/4096$	Typ+20	mV
Full Scale Transition Voltage 6)	V_{FST}	-	Between 4094 and 4095	Typ-20	$V_{rh}-(V_{rh}-V_{rl})/4096$	Typ+20	mV
Integral Non Linearity 7)	INL	-	End point method	−4	-	4	LSB
Differential Non Linearity 7)	DNL	-	End point method	−4	-	4	LSB

6) VZT and VFST are dependent on chip LAYOUT and wiring resistance.
VZT and VFST are dependent on output impedance of the driver drives VIN (Rimp).
The relation between VZT / VFST and Rimp is shown in Table 2.17 .

7) 1LSB=(VFST−VZT)/4094, INLn=(Vn−(1LSB×(n−1)+VZT))/1LSB, DNLn=(Vn+1−Vn)/1LSB−1
INL is dependent on output impedance of the driver drives VIN (Rimp).
The relation between INL and Rimp is shown in Table 2.18 .

Table 2.17. : Relation between VZT/VFST and Rimp

Rimp(ohm)	VZT			VFST		
	Min	Typ	Max	Min	Typ	Max
1000	Typ−20	$V_{RL}+(V_{RH}-V_{RL})/4096$	Typ+20	Typ−20	$V_{RH}-(V_{RH}-V_{RL})/4096$	Typ+20
10000	Typ−30	$V_{RL}+(V_{RH}-V_{RL})/4096$	Typ+20	Typ−20	$V_{RH}-(V_{RH}-V_{RL})/4096$	Typ+25
100000	Typ−100	$V_{RL}+(V_{RH}-V_{RL})/4096$	Typ+20	Typ−20	$V_{RH}-(V_{RH}-V_{RL})/4096$	Typ+50

Table 2.18. : Relation between INL and Rimp

Rimp(ohm)	INL		
	Min	Typ	Max
1000	−5	-	5
10000	−8	-	8
100000	−38	-	38

2.4.4. SSCG I/O

Table 2.19. : Recommended operating conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power voltage	V	-	1.1	1.2	1.3	V
Junction temperature	T_j	-	–40	25	125	°C
Reference clock frequency	F_{ref}	MB86R11F	20	-	50	MHz
		MB86R12/13	10	-	50	
Input clock rise time	t_r	-	-	-	0.4	ns
Input clock fall time	t_f	-	-	-	0.4	ns
Input clock pulse width	T_{high}	High pulse	1.5	-	-	ns
	T_{low}	Low pulse	1.5	-	-	ns
Reset enable time	T_{reset}	-	3	-	-	us

These Recommended SSCG PLL Operation Conditions are settled to guarantee correct operation of SSCG PLL. SSCG PLL Spec (Table 2.20) is guaranteed under the recommended PLL operation conditions.

Table 2.20. : SSCG characteristic

	Parameter	Symbol	Specification			Unit
			Min	Typ	Max	
1	Lock-up Time	T_L	-		200	us
2	Current Consumption	I_{avd}	-	2	4	mA
3	Stand-by Current	I_{off_avd}	-	3	500	uA
4	Output frequency	F_{core}	400	-	1600	MHz
5	VCO Output frequency	F_{out}	800	-	1600	MHz
6	Modulation rate	Om	0.5		5[1)]	%
7	Modulation frequency	F_{mod}	Fref/4096		Fref/1024[2)]	Hz

Note:

- The values are specified under the condition that Power Supply has no noise.
- In this PLL, VCO does not oscillate free-running. The output frequency of SSCG PLL becomes 0Hz when input clock CK is assumed to be 0Hz. Moreover, SSCG PLL operation at this time (CK=0Hz) is not guaranteed

1) Depends on multiples.

Multiple	MAX modulation rate
8 –120	1%
8 – 96	2%
8 – 62	3%
8 – 46	4%
8 – 36	5%

2) Depends on Input frequency

F_{ref}	MAX modulation frequency
10 – 25MHz	F_{ref} /1024
25 – 50MHz	F_{ref} /2048

2.4.4.1. PLL Clock Jitter

PLL clock jitter is calculated by the following formula.

Please confirm the permissible input jitter of the outer module to its manufacturer.

(1) Modulation Off

* CRG_P or SSCGCTL.SSEN=0 (CCNT Register)

f:PLL frequency

n:divide

(1-a) CRPLC.PSMODE=1 (CRG Register)

Jitter=0.03*sqrt(n)/f [sec]

(1-b) CRPLC.PSMODE=0 (CRG Register)

Jitter=0.05*sqrt(n)/f [sec]

(2) Modulation On

* SSCGCTL.SSEN=1(CCNT Register)

f:PLL frequency

n:divide

(2-a) CRPLC.PSMODE=1(CRG Register)

Jitter=0.03*n/f [sec]

(2-b) CRPLC.PSMODE=0(CRG Register)

Jitter=0.05*n/f [sec]

Example:

SSCGCTL.SSEN=1(Modulation On)

CRPLC.PSMODE=1

Modulation rate 0.5%

PLL frequency 1600MHz

Calculation CLK0(400MHz) Jitter

Jitter=0.03*4/(1600*10^6)=75*10^(-12)=75[ps]

Modulation=12.5[ps] 0.5% of 400MHz

Jitter'=Modulattion+Jitter=12.5[ps]+75[ps]=87.5[ps]

2.4.4.2. Difference permission level of crystal (MB86R11F)

Make the difference between CLKX0 and CLKX1 less than 100ps.

2.4.5. I²C Bus Fast Mode I/O

Table 2.21. : I2C I/O direct current characteristic

Parameter & Condition	Symbol	Standard Mode		Fast Mode(*1)		Unit
		Min	Max	Min	Max	
"L" level input voltage	V_{IL}	−0.5	0.3 VDDE	−0.5	0.3 VDDE	V
"H" level input voltage	V_{IH}	0.7 VDDE	2)	0.7 VDDE	2)	V
Schmitt trigger hysteresis VDDE > 2[v]	V_{hys}	n/a	n/a	0.05 VDDE	-	V
"L" level output voltage Sink current 3[mA] VDDE > 2[V]	VOL1	0	0.4	0	0.4	V
Output slew rate (T_{fall}) Bus capacitance 10[pF] ~ 400[pF] V_{IH} (min.) to V_{IL} (max.)	tof	-	250	20 + 0.1Cb 3)	250	ns
Data line leakage Input voltage 0.1 ~ 0.9 VDDE (max.)	I_i	−10	10	-10	10	μA
I/O pin capacitance	C_i	-	10	-	10	pF

1) This I2C Bus Fast Mode I/O buffer is downward compatible with Standard Mode.
2) 65nm technology: Complies with the maximum ratings 4[V].
3) C_b: Capacitance of one bus line [pF)]
4) The I2C Bus Fast Mode I/O Buffer itself has no function to prevent a spike of 50ns pulse width (max).
Therefore, provide any input filter to prevent a spike for both internal or external semiconductor device.

Note: An external pin in the I2C IO buffer is as follows.
I2C0_SCL → I2C0_SDA → I2C1_SCL → I2C1_SDA

2.4.5.1. I2C IO V-I Characteristic Chart

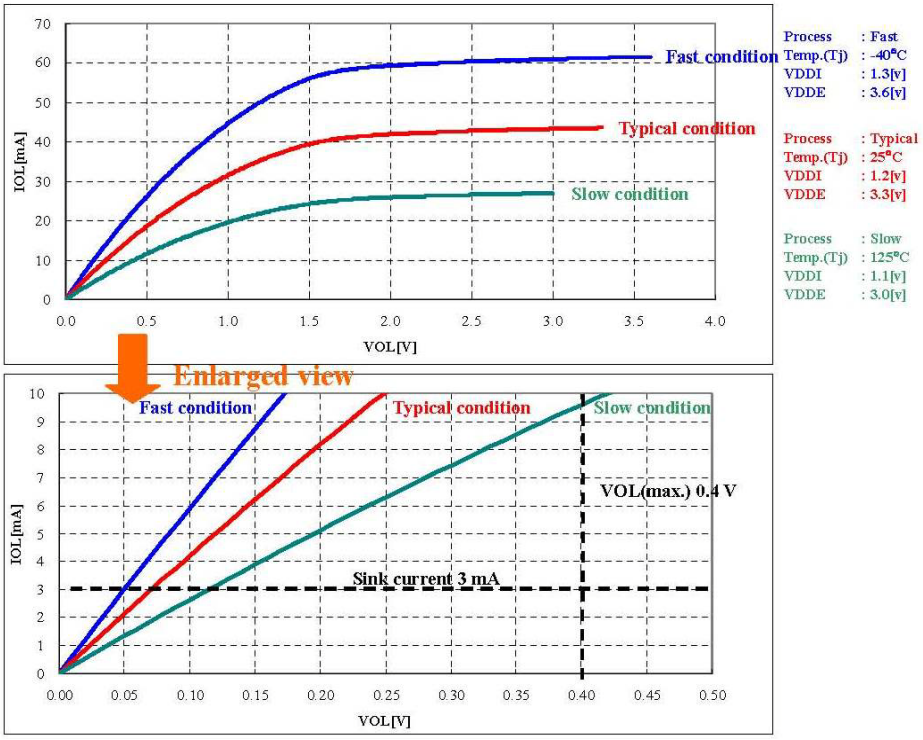


Figure 2.10. : I2C V-I characteristic chart

2.4.6. RSDS I/O

Table 2.22 shows the standard RSDS I/O characteristics valid only for Differential Mode

For Non-Differential Mode, refer to Table 2.10 Standard CMOS I/O DC characteristics.

Table 2.22. : Standard RSDS I/O characteristics

Parameter		Target			Units	Comments
		Min	Typ	Max		
Output differential voltage amplitude, RSDS mode (Vd)	MB86R11F	100	200	600	mV	1. BOOST0=1, RL=50Ω 2. BOOST0=0, RL=100Ω
	MB86R12/13	100	200	300		
Output common voltage, RSDS mode (Vcm)	MB86R11F	0.5	1.2	1.5	V	Some RSDS receivers require Vcm<1.3V in corner cases.
	MB86R12/13	1	1.2	1.55		
Output current amplitude, RSDS mode (Iload)	MB86R11F	1	2	6	mA	BOOST0=0 RL=100Ω
	MB86R12/13	1	2	3		
Output current amplitude, RSDS mode (Iload)	MB86R11F	2	4	6	mA	BOOST0=1 RL=50Ω
	MB86R12/13					

2.4.7. USB I/O

Table 2.23. : Recommended operating conditions (High-speed)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input levels for high-speed:					
high-speed squelch detection threshold (differential signal amplitude)	VHSSQ	100	-	200	mV
High-speed disconnect detection threshold (differential signal amplitude)	VHSDSC	525	-	625	mV
High-speed differential input signaling levels (this spec is based on "Template 6")		150 (absolute value)	-	-	mV
High-speed data signaling common mode voltage range (guideline for receiver)	VHSCM	-50	-	500	mV
Output levels for high-speed:					
High-speed idle level	VHSOI	-10.0	-	10.0	mV
High-speed data signaling high	VHSOH	360	-	440	mV
High-speed data signaling low	VHSOL	-10.0	-	10.0	mV
Chirp J level (differential voltage)	VCHIRPJ	700	-	1100	mV
Chirp K level (differential voltage)	VCHIRPK	-900	-	-500	mV
Terminations in high-speed:					
Termination voltage in high-speed	VHSTERM	-10	-	10	mV

Table 2.24. : Recommended operating conditions (Full-speed/Low-speed)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input levels for full-speed/low-speed:					
High (driving)	VIH	2.0	-	-	V
High (floating)	VIHZ	2.7	-	3.6	V
Low	VIL	-	-	0.8	V
Differential input sensitivity	VDI	0.2	-	-	V
Differential common mode range	VCM	0.8	-	2.5	V
Output levels for full-speed/low-speed:					
Low	VOL	0.0	-	0.3	V
High (driven)	VOH	2.8	-	3.6	V
SE1	VOSE1	0.8	-	-	V
Output signal crossover voltage	VCRS	1.3	-	2.0	V
Input capacitance for full-speed/low-speed:					
Downstream facing port (being shared with upstream facing port at device mode, so the less value is selected as the maximum spec)	CIND (CINUB)	-	-	100	pF

Table 2.24. : Recommended operating conditions (Full-speed/Low-speed)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Transceiver edge rate control capacitance	CEDGE	-	-	75	pF
Terminations in full-speed/low-speed:					
Bus pull-up resistor on upstream port (idle bus) (this is used only in the device mode (HOST-MODE = "0" setting).)	RPUI	0.9	-	1.575	kΩ
Bus pull-up resistor on upstream port (upstream port receiving) (this is used only in the device mode (HOSTMODE = "0" setting).)	RPUA	1.425	-	3.090	kΩ
Input impedance exclusive of pull-up/pull-down	ZINP	300	-	-	kΩ
Termination voltage on upstream port pull-up	VTERM	3.0	-	3.6	V

2.5. AC Characteristics

This chapter explains the AC timing of external terminals.

2.5.1. External Bus Controller Signal Timing

Table 2.25. : Memory controller signal timing

Signal Name	Symbol	Description	Value			Unit
			Min	Typ	Max	
MB86R11F: MEM_XCS[0,1,2] MB86R12/13: MEM_XCS[0,2,4]	T_{cso}	Chip Select delay time	-	-	13	ns
MEM_EA[26:1]	T_{ao}	Address delay time	-	-	13	ns
MEM_ED[31:0]	T_{do}	Data output delay time	-	-	13	ns
	T_{doz}	Data output HiZ time	-	-	13	ns
	T_{dsr}	SRAM/NOR Flash data setup time	13.5	-	-	ns
	T_{dhr}	SRAM/NOR Flash data hold time	0	-	-	ns
	T_{dsp}	NOR Flash page Read data setup time	13.5	-	-	ns
	T_{dhp}	NOR Flash page Read data hold time	0	-	-	ns
MEM_RDY	T_{dri}	RDY delay time	0.5	-	-	ns
MEM_XRD	T_{rdo}	XRD delay time	-	-	13	ns
MEM_XWR[3:0]	T_{wro}	XWR delay time	-	-	13	ns

Output Delay's standard clock is an internal clock.
A standard clock of MEM_RDY is an internal clock.
T_{RACC}: Timing Register[3:0].RACC[3:0]
T_{RADC}: Timing Register[7:4].RADC[3:0]
T_{WADC}: Timing Register[23:20].WADC[3:0]

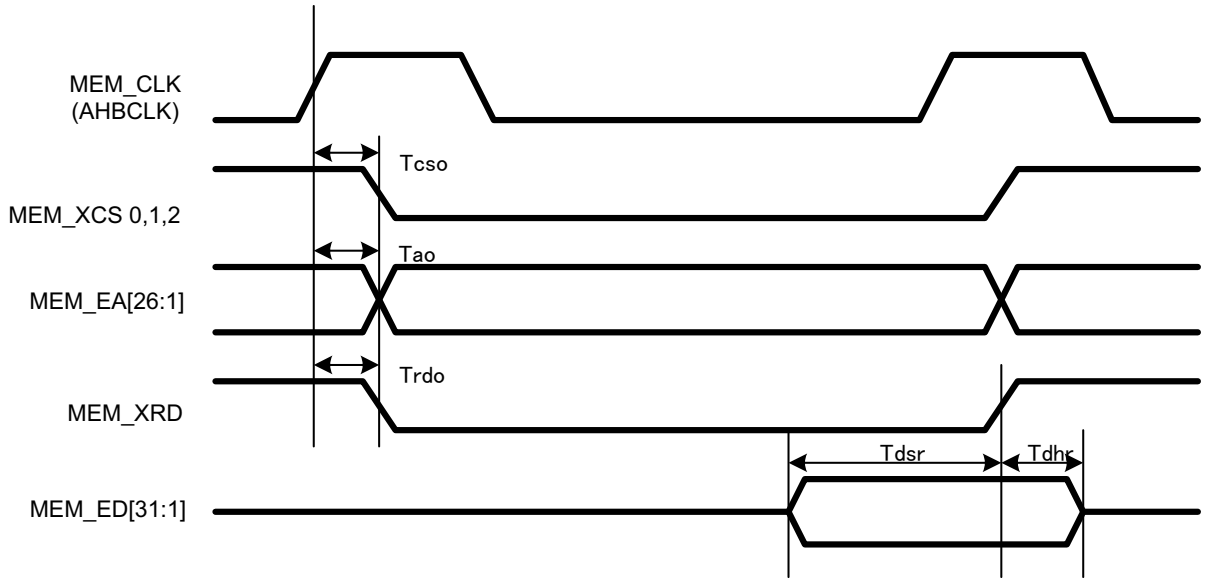


Figure 2.11. : SRAM/NOR Flash Read

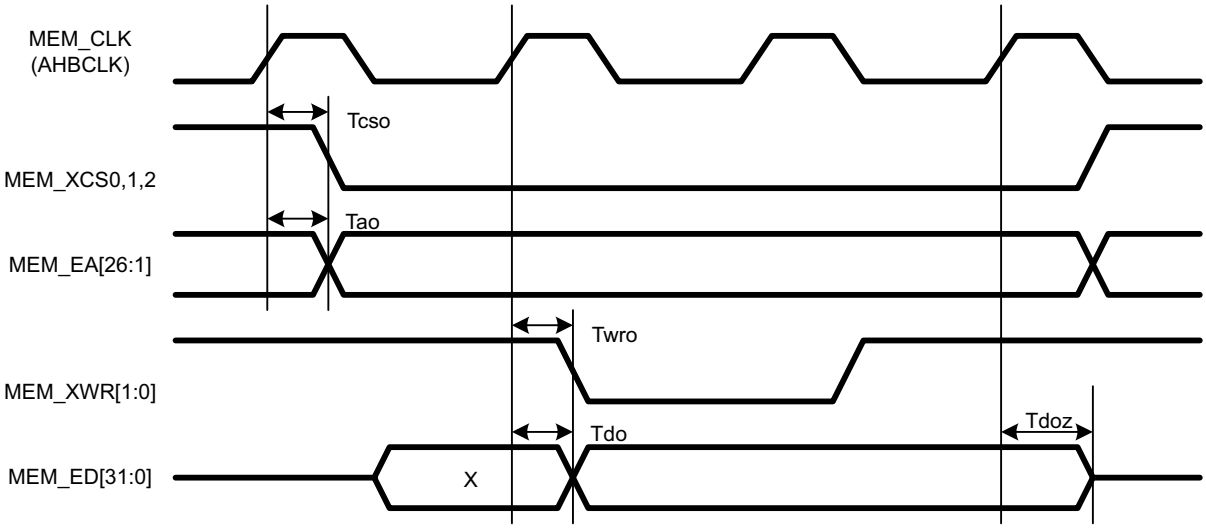


Figure 2.12. : SRAM/NOR Flash Write

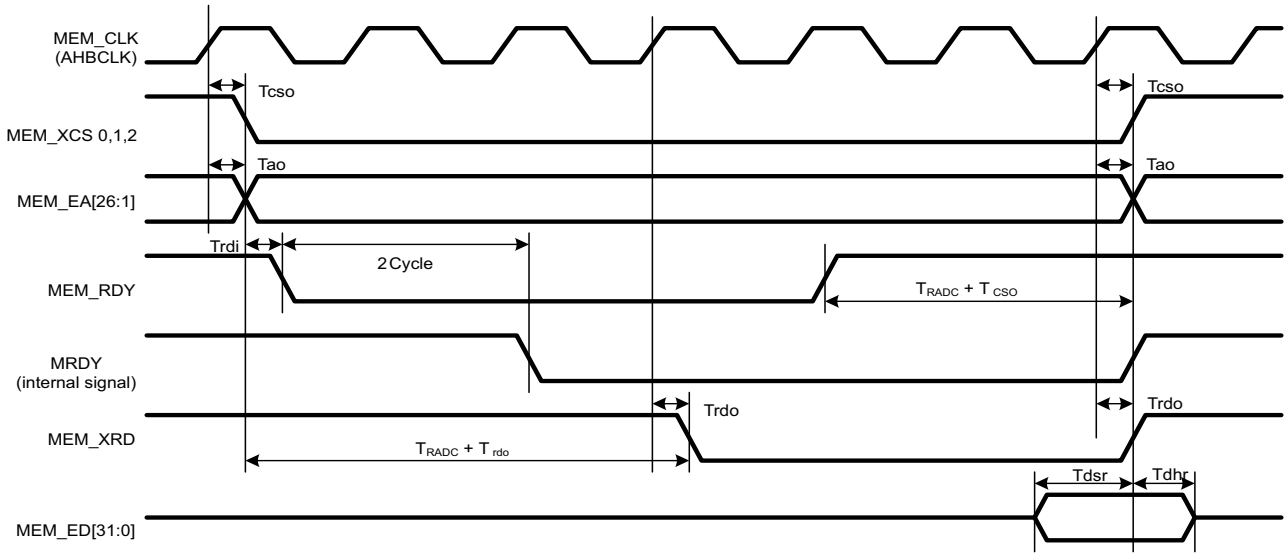


Figure 2.13. : Low speed device Read

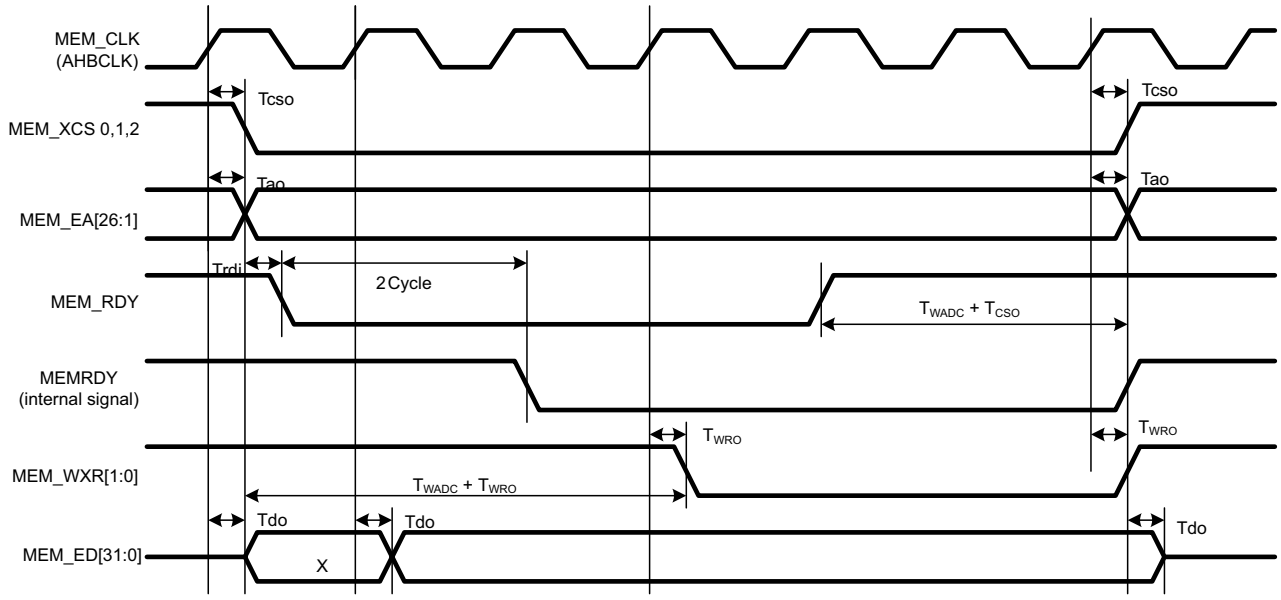


Figure 2.14. : Low speed device Write

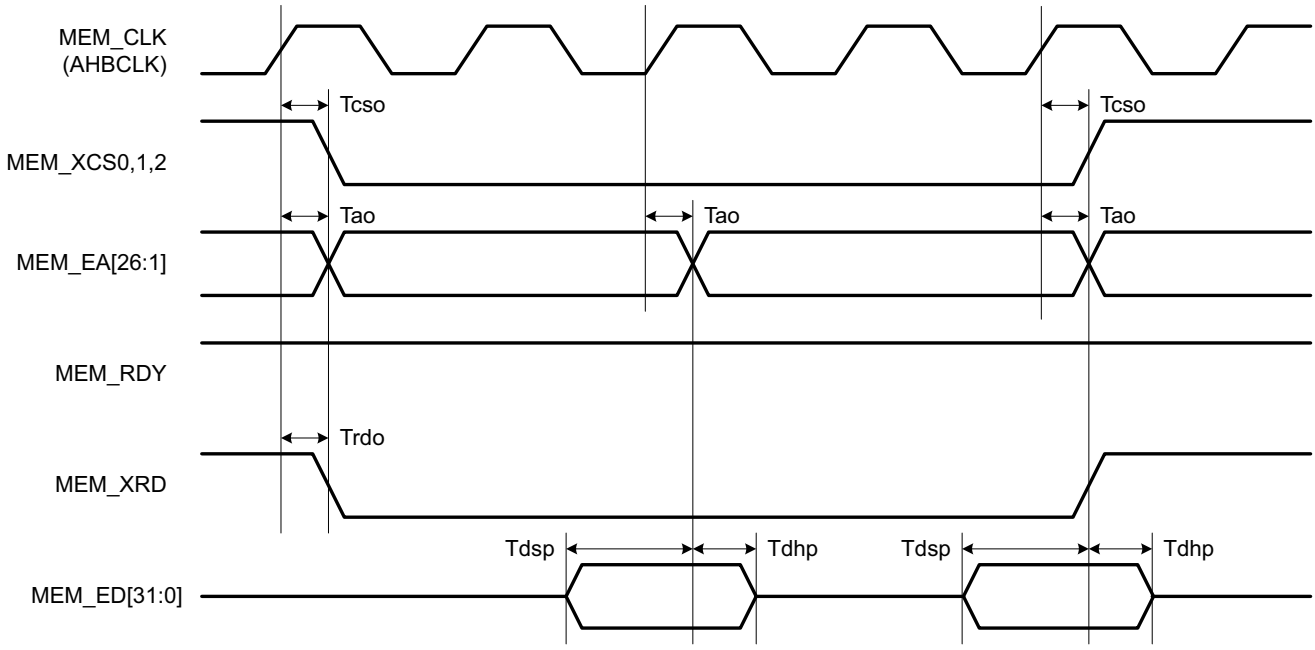


Figure 2.15. : NOR Flash Page Read

2.5.2. DDR Controller Signal Timing

Table 2.26. : DDR Controller(DDR3-1066) signal timing by SSTL15 mode

Signal Name	Symbol	Description	Value		Unit
			Min	Max	
MA* MBA*, MCKE, MODT, MXCAS, MXCS, MXRAS, MXWE	tphy_IS_CA	Control and Address setup time	-	737	ps
	tphy_IH_CA	Control and Address hold time	-	410	ps
MDQS0, MXDQS0	tphy_CKDQS_min	DQS output access time from CLK	−474	-	ps
	tphy_CKDQS_max	DQS output access time from CLK	-	284	ps
	tphy_RTT_Gate_min	Round Trip time from CLK out to Read DQS	240	-	ps
	tphy_RTT_Gate_max	Round Trip time from CLK out to Read DQS	-	955	ps
MDQS1, MXDQS1	tphy_CKDQS_min	DQS output access time from CLK	−468	-	ps
	tphy_CKDQS_max	DQS output access time from CLK	-	288	ps
	tphy_RTT_Gate_min	Round Trip time from CLK out to Read DQS	244	-	ps
	tphy_RTT_Gate_max	Round Trip time from CLK out to Read DQS	-	956	ps
MDQS2, MXDQS2	tphy_CKDQS_min	DQS output access time from CLK	−311	-	ps
	tphy_CKDQS_max	DQS output access time from CLK	-	440	ps
	tphy_RTT_Gate_min	Round Trip time from CLK out to Read DQS	364	-	ps
	tphy_RTT_Gate_max	Round Trip time from CLK out to Read DQS	-	1092	ps
MDQS3, MXDQS3	tphy_CKDQS_min	DQS output access time from CLK	−316	-	ps
	tphy_CKDQS_max	DQS output access time from CLK	-	434	ps
	tphy_RTT_Gate_min	Round Trip time from CLK out to Read DQS	359	-	ps
	tphy_RTT_Gate_max	Round Trip time from CLK out to Read DQS	-	1084	ps
MDQ[7:0], MDM0	tphy_WDS	DQ and DM setup time for Write	-	306	ps
	tphy_WDH	DQ and DM hold time for Write	-	313	ps
	tphy_RDS	DQ and DM setup time for Read	-	278	ps
	tphy_RDH	DQ and DM hold time for Read	622	-	ps
MDQ[15:8], MDM1	tphy_WDS	DQ and DM setup time for Write	-	306	ps
	tphy_WDH	DQ and DM hold time for Write	-	312	ps
	tphy_RDS	DQ and DM setup time for Read	-	278	ps
	tphy_RDH	DQ and DM hold time for Read	622	-	ps
MDQ[23:16], MDM2	tphy_WDS	DQ and DM setup time for Write	-	306	ps
	tphy_WDH	DQ and DM hold time for Write	-	313	ps
	tphy_RDS	DQ and DM setup time for Read	-	277	ps
	tphy_RDH	DQ and DM hold time for Read	621	-	ps

Table 2.26. : DDR Controller(DDR3-1066) signal timing by SSTL15 mode (Continued)

Signal Name	Symbol	Description	Value		Unit
			Min	Max	
MDQ[31:24], MDM3	tphy_WDS	DQ and DM setup time for Write	-	306	ps
	tphy_WDH	DQ and DM hold time for Write	-	310	ps
	tphy_RDS	DQ and DM setup time for Read	-	278	ps
	tphy_RDH	DQ and DM hold time for Read	623	-	ps
MDQS0, MXDQS0	t_phy_RTT_FIFO_min	Round Trip time from CLK out to Read DQS for Read data synchronizer	–246	-	ps
	t_phy_RTT_FIFO_max	Round Trip time from CLK out to Read DQS for Read data synchronizer	-	1831	ps
MDQS1, MXDQS1	t_phy_RTT_FIFO_min	Round Trip time from CLK out to Read DQS for Read data synchronizer	–245	-	ps
	t_phy_RTT_FIFO_max	Round Trip time from CLK out to Read DQS for Read data synchronizer	-	1837	ps
MDQS2, MXDQS2	t_phy_RTT_FIFO_min	Round Trip time from CLK out to Read DQS for Read data synchronizer	–266	-	ps
	t_phy_RTT_FIFO_max	Round Trip time from CLK out to Read DQS for Read data synchronizer	-	1790	ps
MDQS3, MXDQS3	t_phy_RTT_FIFO_min	Round Trip time from CLK out to Read DQS for Read data synchronizer	–262	-	ps
	t_phy_RTT_FIFO_max	Round Trip time from CLK out to Read DQS for Read data synchronizer	-	1809	ps

Table 2.27. : DDR Controller(DDR3-800) signal timing by SSTL15 mode

Signal Name	Symbol	Description	Value		Unit
			Min	Max	
MA* MBA*, MCKE, MODT, MXCAS, MXCS, MXRAS, MXWE	tphy_IS_CA	Control and Address setup time	-	1034	ps
	tphy_IH_CA	Control and Address hold time	-	714	ps
MDQS0, MXDQS0	tphy_CKDQS_min	DQS output access time from CLK	–501	-	ps
	tphy_CKDQS_max	DQS output access time from CLK	-	311	ps
	tphy_RTT_Gate_min	Round Trip time from CLK out to Read DQS	–36	-	ps
	tphy_RTT_Gate_max	Round Trip time from CLK out to Read DQS	-	1250	ps
MDQS1, MXDQS1	tphy_CKDQS_min	DQS output access time from CLK	–495	-	ps
	tphy_CKDQS_max	DQS output access time from CLK	-	315	ps
	tphy_RTT_Gate_min	Round Trip time from CLK out to Read DQS	–32	-	ps
	tphy_RTT_Gate_max	Round Trip time from CLK out to Read DQS	-	1251	ps

Table 2.27. : DDR Controller(DDR3-800) signal timing by SSTL15 mode (Continued)

Signal Name	Symbol	Description	Value		Unit
			Min	Max	
MDQS2, MXDQS2	tphy_CKDQS_min	DQS output access time from CLK	−348	-	ps
	tphy_CKDQS_max	DQS output access time from CLK	-	457	ps
	tphy_RTT_Gate_min	Round Trip time from CLK out to Read DQS	69	-	ps
	tphy_RTT_Gate_max	Round Trip time from CLK out to Read DQS	-	1367	ps
MDQS3, MXDQS3	tphy_CKDQS_min	DQS output access time from CLK	−363	-	ps
	tphy_CKDQS_max	DQS output access time from CLK	-	441	ps
	tphy_RTT_Gate_min	Round Trip time from CLK out to Read DQS	93	-	ps
	tphy_RTT_Gate_max	Round Trip time from CLK out to Read DQS	-	1388	ps
MDQ[7:0], MDM0	tphy_WDS	DQ and DM setup time for Write	-	448	ps
	tphy_WDH	DQ and DM hold time for Write	-	471	ps
	tphy_RDS	DQ and DM setup time for Read	-	420	ps
	tphy_RDH	DQ and DM hold time for Read	776	-	ps
MDQ[15:8], MDM1	tphy_WDS	DQ and DM setup time for Write	-	447	ps
	tphy_WDH	DQ and DM hold time for Write	-	471	ps
	tphy_RDS	DQ and DM setup time for Read	-	420	ps
	tphy_RDH	DQ and DM hold time for Read	776	-	ps
MDQ[23:16], MDM2	tphy_WDS	DQ and DM setup time for Write	-	448	ps
	tphy_WDH	DQ and DM hold time for Write	-	471	ps
	tphy_RDS	DQ and DM setup time for Read	-	419	ps
	tphy_RDH	DQ and DM hold time for Read	776	-	ps
MDQ[31:24], MDM3	tphy_WDS	DQ and DM setup time for Write	-	448	ps
	tphy_WDH	DQ and DM hold time for Write	-	469	ps
	tphy_RDS	DQ and DM setup time for Read	-	420	ps
	tphy_RDH	DQ and DM hold time for Read	778	-	ps
MDQS0, MXDQS0	t_phy_RTT_FIFO_min	Round Trip time from CLK out to Read DQS for Read data synchronizer	−1308	-	ps
	t_phy_RTT_FIFO_max	Round Trip time from CLK out to Read DQS for Read data synchronizer	-	1975	ps
MDQS1, MXDQS1	t_phy_RTT_FIFO_min	Round Trip time from CLK out to Read DQS for Read data synchronizer	−1307	-	ps
	t_phy_RTT_FIFO_max	Round Trip time from CLK out to Read DQS for Read data synchronizer	-	1981	ps
MDQS2, MXDQS2	t_phy_RTT_FIFO_min	Round Trip time from CLK out to Read DQS for Read data synchronizer	−1328	-	ps
	t_phy_RTT_FIFO_max	Round Trip time from CLK out to Read DQS for Read data synchronizer	-	1934	ps
MDQS3, MXDQS3	t_phy_RTT_FIFO_min	Round Trip time from CLK out to Read DQS for Read data synchronizer	−1324	-	ps
	t_phy_RTT_FIFO_max	Round Trip time from CLK out to Read DQS for Read data synchronizer	-	1953	ps

Table 2.28. : DDR Controller(DDR2-800) signal timing by SSTL18 mode

Signal Name	Symbol	Description	Value		Unit
			Min	Max	
MA* MBA*, MCKE, MODT, MXCAS, MXCS, MXRAS, MXWE	tphy_IS_CA	Control and Address setup time	-	1053	ps
	tphy_IH_CA	Control and Address hold time	-	740	ps
MDQS0, MXDQS0	tphy_CKDQS_min	DQS output access time from CLK	–496	-	ps
	tphy_CKDQS_max	DQS output access time from CLK	-	297	ps
	tphy_RTT_Gate_min	Round Trip time from CLK out to Read DQS	26	-	ps
	tphy_RTT_Gate_max	Round Trip time from CLK out to Read DQS	-	1357	ps
MDQS1, MXDQS1	tphy_CKDQS_min	DQS output access time from CLK	–490	-	ps
	tphy_CKDQS_max	DQS output access time from CLK	-	301	ps
	tphy_RTT_Gate_min	Round Trip time from CLK out to Read DQS	30	-	ps
	tphy_RTT_Gate_max	Round Trip time from CLK out to Read DQS	-	1358	ps
MDQS2, MXDQS2	tphy_CKDQS_min	DQS output access time from CLK	–342	-	ps
	tphy_CKDQS_max	DQS output access time from CLK	-	443	ps
	tphy_RTT_Gate_min	Round Trip time from CLK out to Read DQS	131	-	ps
	tphy_RTT_Gate_max	Round Trip time from CLK out to Read DQS	-	1473	ps
MDQS3, MXDQS3	tphy_CKDQS_min	DQS output access time from CLK	–357	-	ps
	tphy_CKDQS_max	DQS output access time from CLK	-	427	ps
	tphy_RTT_Gate_min	Round Trip time from CLK out to Read DQS	155	-	ps
	tphy_RTT_Gate_max	Round Trip time from CLK out to Read DQS	-	1495	ps
MDQ[7:0], MDM0	tphy_WDS	DQ and DM setup time for Write	-	432	ps
	tphy_WDH	DQ and DM hold time for Write	-	382	ps
	tphy_RDS	DQ and DM setup time for Read	-	363	ps
	tphy_RDH	DQ and DM hold time for Read	844	-	ps
MDQ[15:8], MDM1	tphy_WDS	DQ and DM setup time for Write	-	432	ps
	tphy_WDH	DQ and DM hold time for Write	-	382	ps
	tphy_RDS	DQ and DM setup time for Read	-	363	ps
	tphy_RDH	DQ and DM hold time for Read	844	-	ps
MDQ[23:16], MDM2	tphy_WDS	DQ and DM setup time for Write	-	431	ps
	tphy_WDH	DQ and DM hold time for Write	-	382	ps
	tphy_RDS	DQ and DM setup time for Read	-	363	ps
	tphy_RDH	DQ and DM hold time for Read	846	-	ps

Table 2.28. : DDR Controller(DDR2-800) signal timing by SSTL18 mode (Continued)

Signal Name	Symbol	Description	Value		Unit
			Min	Max	
MDQ[31:24], MDM3	tphy_WDS	DQ and DM setup time for Write	-	430	ps
	tphy_WDH	DQ and DM hold time for Write	-	381	ps
	tphy_RDS	DQ and DM setup time for Read	-	363	ps
	tphy_RDH	DQ and DM hold time for Read	848	-	ps
MDQS0, MXDQS0	t_phy_RTT_FIFO_min	Round Trip time from CLK out to Read DQS for Read data synchronizer	–1206	-	ps
	t_phy_RTT_FIFO_max	Round Trip time from CLK out to Read DQS for Read data synchronizer	-	2238	ps
MDQS1, MXDQS1	t_phy_RTT_FIFO_min	Round Trip time from CLK out to Read DQS for Read data synchronizer	–1205	-	ps
	t_phy_RTT_FIFO_max	Round Trip time from CLK out to Read DQS for Read data synchronizer	-	2244	ps
MDQS2, MXDQS2	t_phy_RTT_FIFO_min	Round Trip time from CLK out to Read DQS for Read data synchronizer	–1226	-	ps
	t_phy_RTT_FIFO_max	Round Trip time from CLK out to Read DQS for Read data synchronizer	-	2197	ps
MDQS3, MXDQS3	t_phy_RTT_FIFO_min	Round Trip time from CLK out to Read DQS for Read data synchronizer	–1222	-	ps
	t_phy_RTT_FIFO_max	Round Trip time from CLK out to Read DQS for Read data synchronizer	-	2216	ps

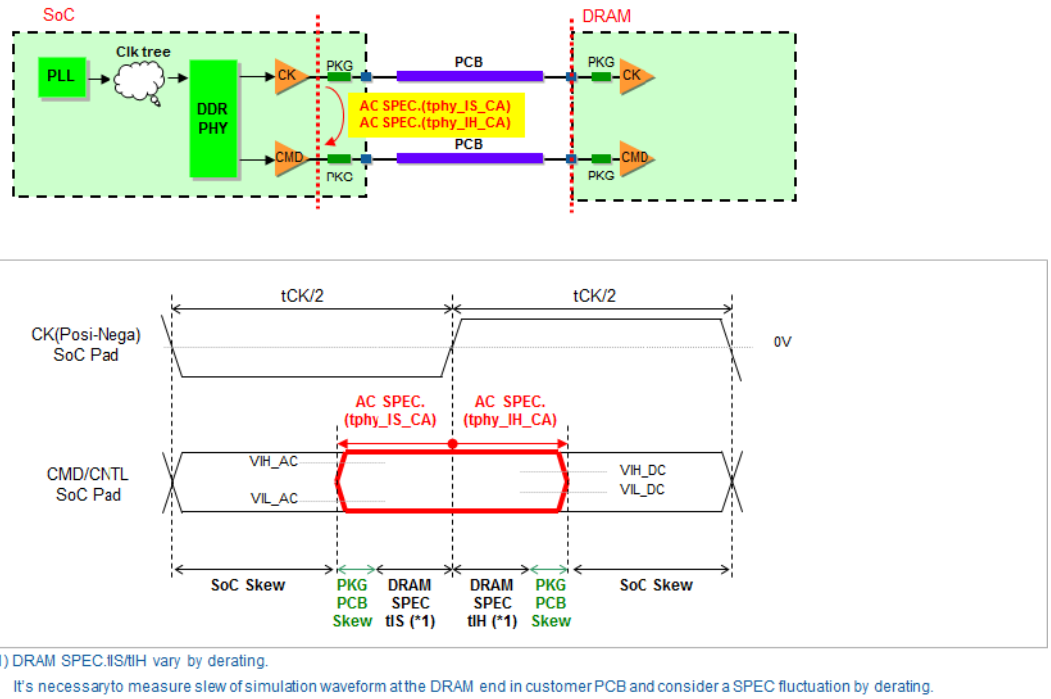


Figure 2.16. : tphy_IS_CA/tphy_IH_CA timing

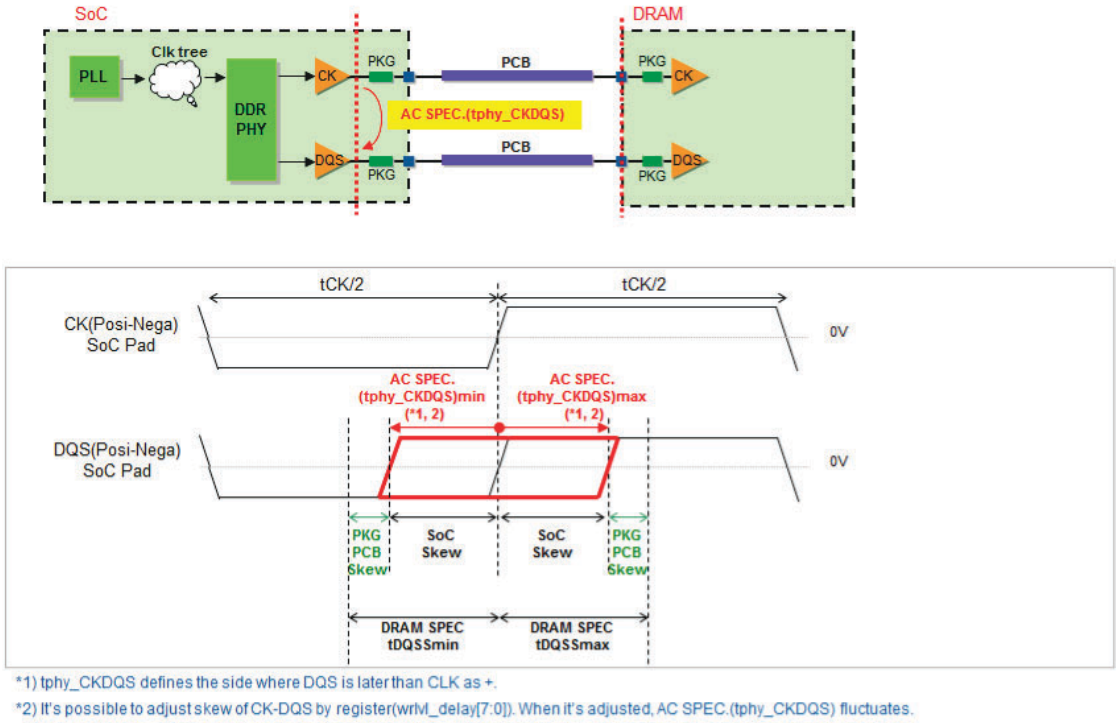


Figure 2.17. : tphy_CKDQS timing #1

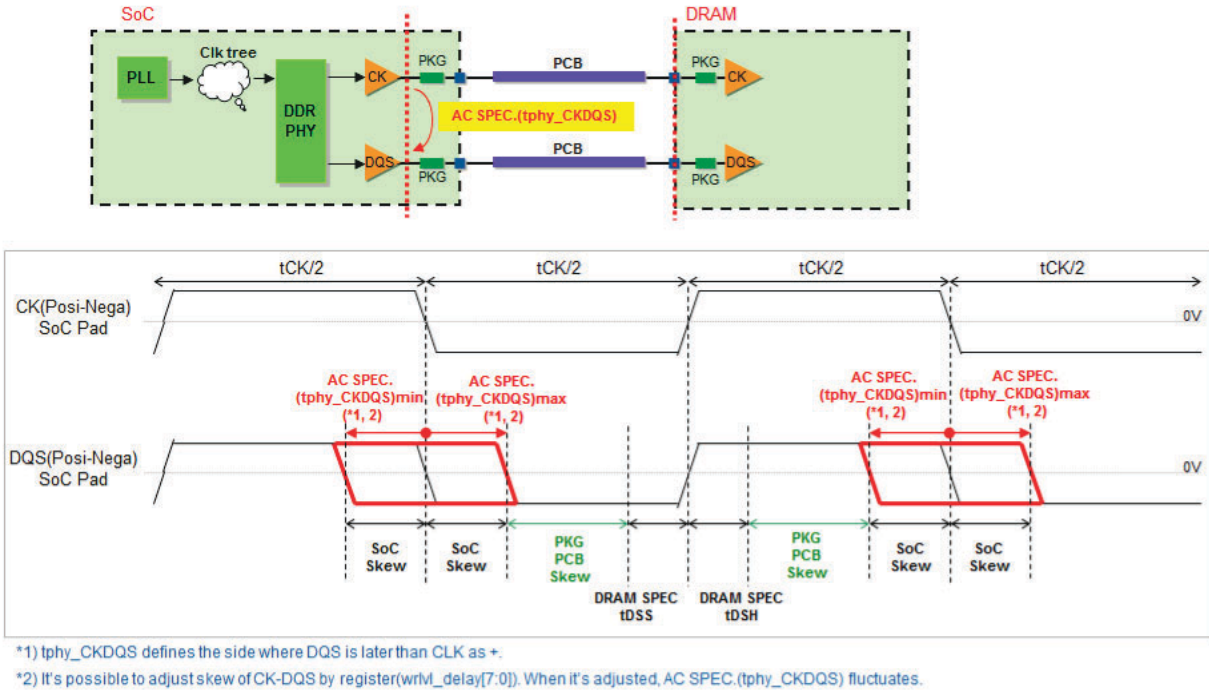


Figure 2.18. : tphy_CKDQS timing #2

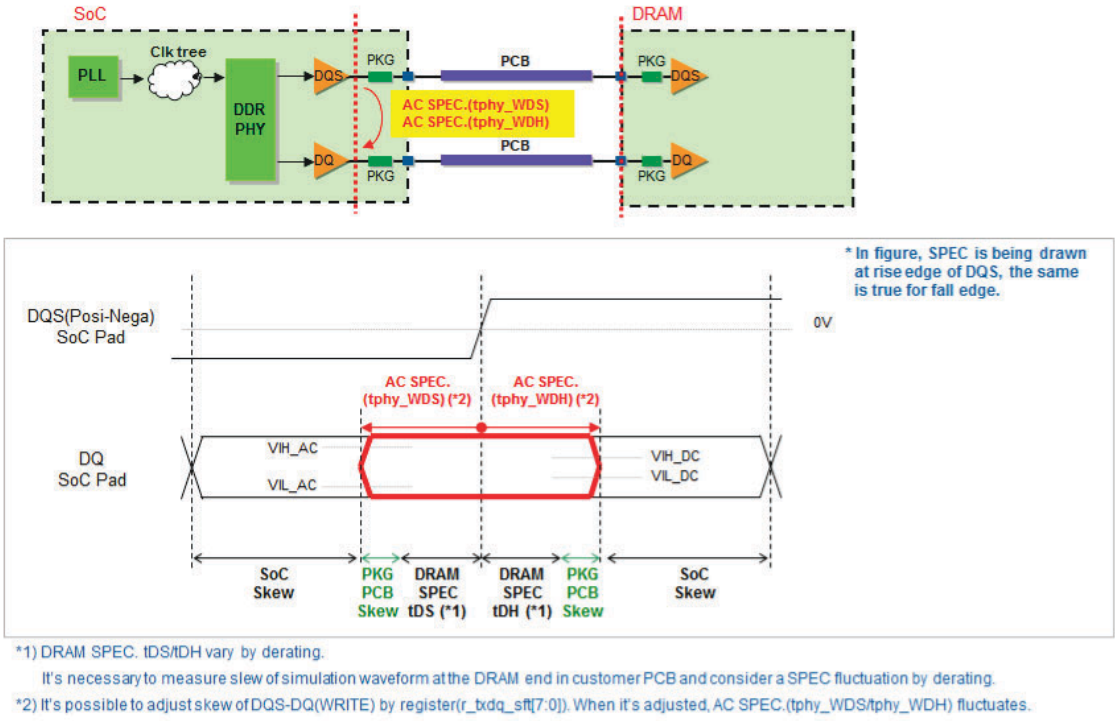


Figure 2.19. : tphy_WDS/tphy_WDH timing

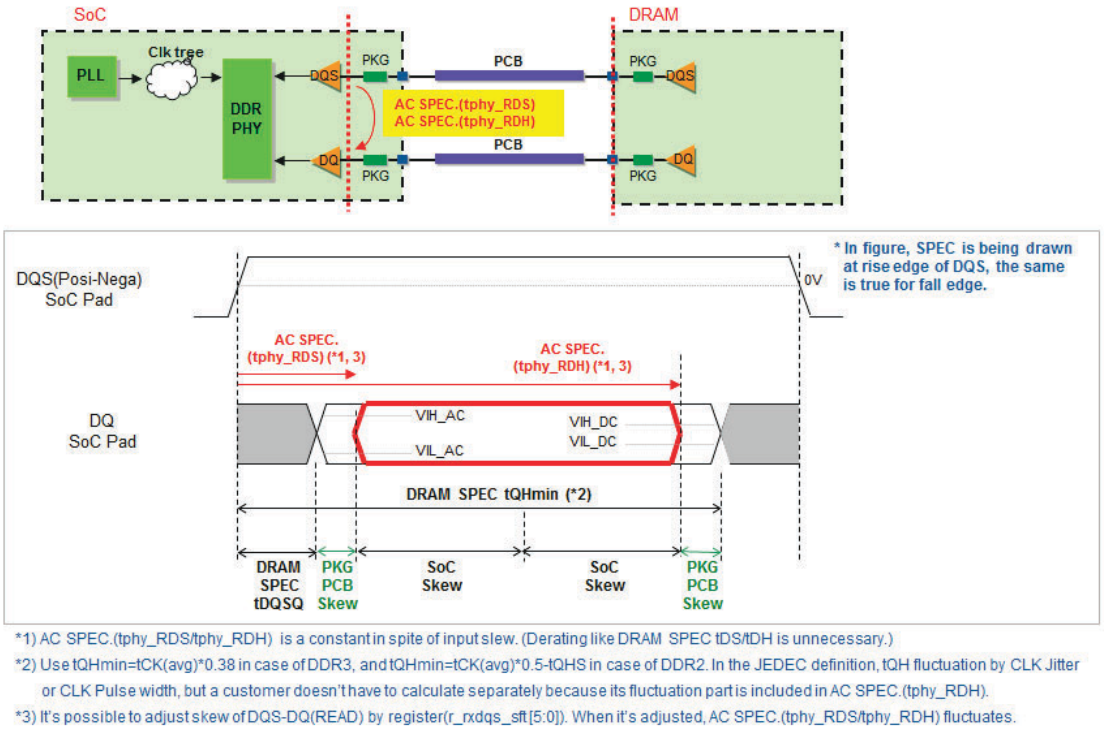


Figure 2.20. : tphy_RDS/tphy_RDH timing

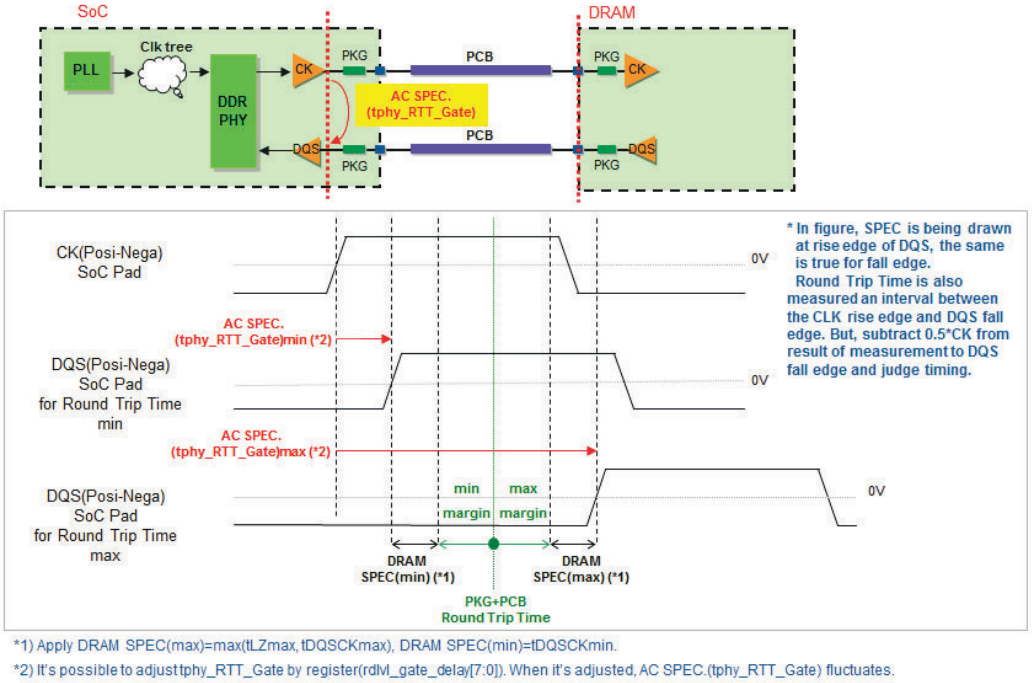


Figure 2.21. : tphy_RTT_Gate timing

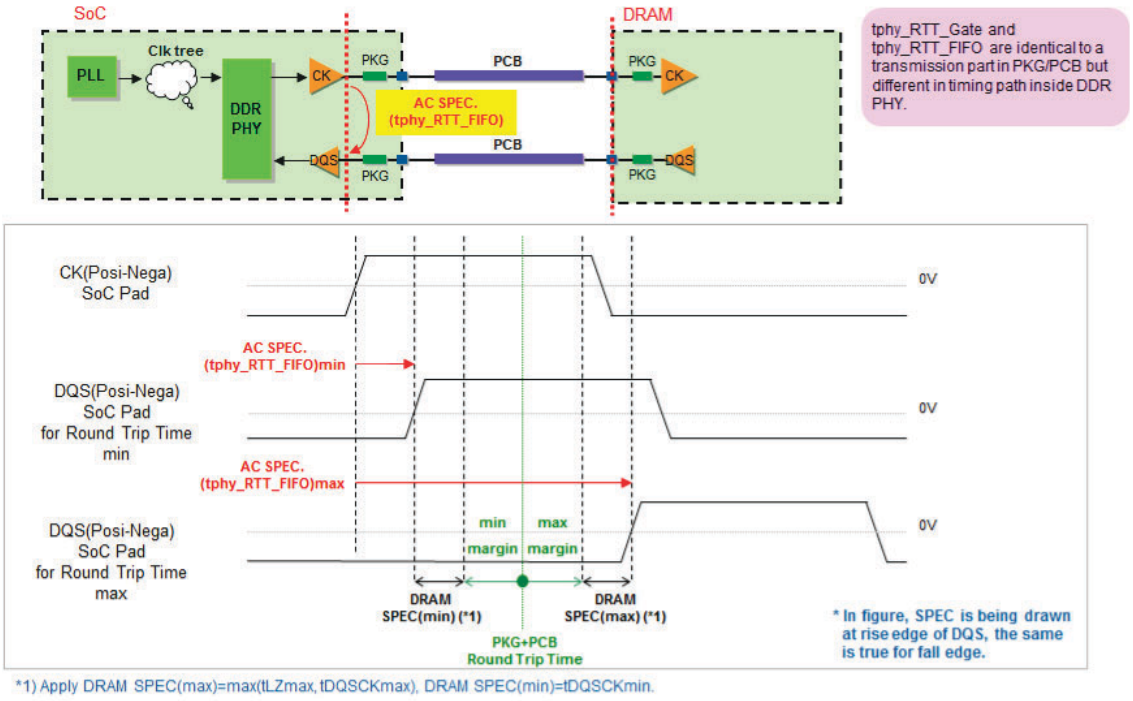


Figure 2.22. : tphy_RTT_FIFO timing

2.5.3. Display Controller Unit Signal Timing

2.5.3.1. Clock

Table 2.29. : AC timing of video interface clock signal

Signal	Symbol	Description	Value			Unit
			Min	Typ	Max	
DISP*n*CLKI	F_{dclki}	DCLKI frequency	-	-	133	MHz
	T_{hdclki}	DCLKI H width	5	-	-	ns
	T_{ldclki}	DCLKI L width	5	-	-	ns
DCLK (internal) 2)	T_{ldclk}	DCLK frequency 1)	-	-	133	MHz
DISP*n*CLKO	F_{dclko}	DCLKO frequency	-	-	133	MHz
DISP*n*CLKO	T_{hdclko}	DCLKO H width	typ–0.7	3)	typ+0.7	ns

1) The internal display clock of PLL synchronous mode is generated with internal PLL of the display clock prescaler.
2) DCLKI or PLL internal display clock is output.
3) H pulse width of DISP*n*CLKO is described as follow.
$T_{hdclko(typ)}$ = (PLL cycle time)*n; dual edge mode
$T_{hdclko(typ)}$ = (PLL cycle time)*n/2; single edge mode, n is even number
$T_{hdclko(typ)}$ = (PLL cycle time)*(n-1)/2; single edge mode, n is odd number
$T_{hdclko(typ)}$ = Thdclki; DISP*n*CLKI is used as DCLK source
n is divide ratio defined by SC field of DCLKConfig register, i.e, n = SC+1
PLL cycle time varies if SSCG is used but does not get shorter than standard cycle time
For faster clock operation, setup time of output data is dominating.

2.5.3.2. Input Signal

- Application only in case of PLL synchronous mode (CKS = 0)(clock output from internal standard clock = PLL)

Table 2.30. : AC timing of video interface input signal(1)

Signal	Symbol	Description	Value			Unit
			Min	Typ	Max	
DISP*n*HSYNC (i)	T_{whsync}	HSYNC input pulse width	3.0	-	-	Clock
DISP*n*VSYNC (i)	T_{wvsync}	VSYNC input pulse width	1	-	-	HSYNC

- Application only in case of DCLKI synchronous mode (CKS = 1)(standard clock = DCLKI)

Table 2.31. : AC timing of video interface input signal(2)

Signal	Symbol	Description	Value			Unit
			Min	Typ	Max	
DISP*n*HSYNC (i)	T_{whsync}	HSYNC input pulse width	3.0	-	-	Clock
	T_{shsync}	HSYNC input setup time	6.0	-	-	ns
	T_{hhsync}	HSYNC input hold time	1.0	-	-	ns
DISP*n*VSYNC (i)	T_{wvsync}	VSYNC input pulse width	1	-	-	HSYNC

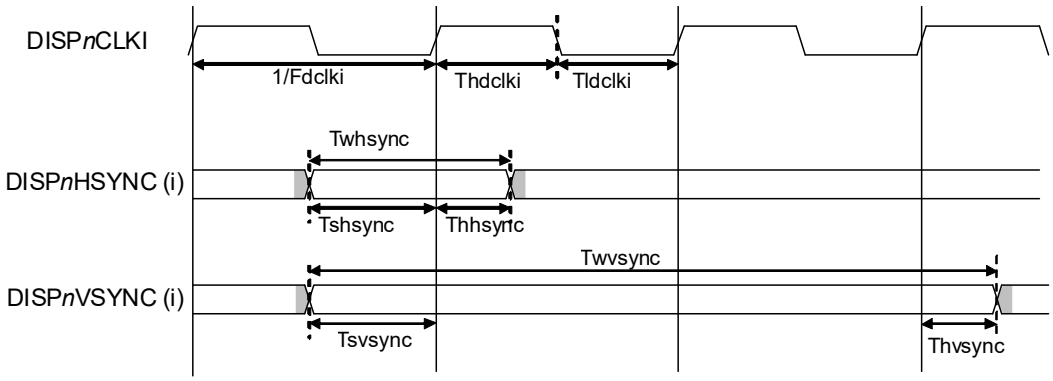


Figure 2.23. : Display input signal timing

2.5.3.3. Output Signal

Table 2.32. : AC timing of video interface output signal

Signal	Symbol	Description	Condition	Value			Unit
				Min	Typ	Max	
DISPLAY CONTROLLER 0							
DISP0R[7:0], DISP0G[7:0], DISP0B[7:0] DISP0HSYNC(o) DISP0VSYNC(o) DISP0DE(o) DISP0CSYNC DISP0GV	T_{drgb0}	RGB output delay time	Single edge mode	0.4	-	5.5	ns
			Dual edge mode	0.4	-	6.0	ns
			Delay mode [1)]	0.4	-	6.0	ns
DISPLAY CONTROLLER 1							
DISP1R[7:0], DISP1G[7:0], DISP1B[7:0] DISP1HSYNC(o) DISP1VSYNC(o) DISP1DE(o) DISP1CSYNC DISP1GV	T_{drgb1}	RGB output delay time	Single edge mode	0.3	-	5.5	ns
			Dual edge mode	0.3	-	6.0	ns
			Delay mode [1)]	0.4	-	6.0	ns
			Dual pixel mode	0.2	-	5.5	ns
DISPLAY CONTROLLER 2							

Table 2.32. : AC timing of video interface output signal

Signal	Symbol	Description	Condition	Value			Unit
				Min	Typ	Max	
DISP2R[7:0], DISP2G[7:0], DISP2B[7:0]	T_{drgb2}	RGB output delay time	Single edge mode	0.4	-	5.5	ns
DISP2HSYNC(o) DISP2VSYNC(o) DISP2DE(o) DISP2CSYNC DISP2GV			Delay mode [1)]	0.4	-	6.0	ns
Single edge mode: DCK edge =0							
Dual edge mode: DCKedge = 1							
Dual pixel mode: DPIX = 1							
Delay mode: DCKdel > 0							
1) digital delay is added to this delay value							
When the holding time is insufficient, reversing the DCLKO clock is recommended.							

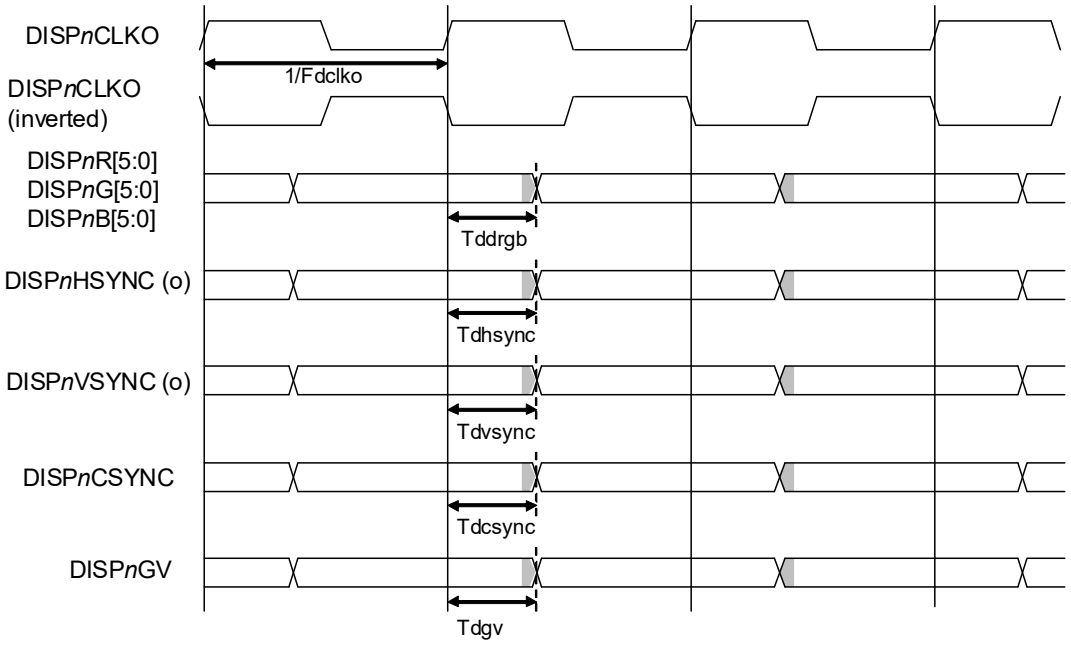


Figure 2.24. : Display output signal timing

The AC characteristic is not defined about the analog signal.

2.5.3.4. TCON Active Display Timing DISP0 Interface

The following values are only valid if the display clock is output at pin DISP0CLKO/DISP0CLKOX, that means ChanSel[i=0..12]=0. If the display clock is output at another pin of DISP0 Interface the timing values might slightly differ.

Note: If TCON is not used, please refer to section“2.5.3.3. Output Signal” as specs of DISPLAY0.

Table 2.33. : AC timing of tcon output signal

Signal	Symbol	Description	Min	Typ	Max	Unit	Condition
RSDS operation mode							
DISP0R[7:0], DISP0G[7:0], DISP0B[7:0]	RSSU	Setup time	1.0	-	-	ns	C_L=10pF, Delay[i]=1 (Data signals), Delay[j]=0 (clock signal)
	RSHD	Hold time	1.0	-	-	ns	C_L=10pF, Delay[i]=1 (Data signals), Delay[j]=0 (clock signal)
DISP0CLKO DISP0CLKOX	f_RSCK	Frequency	-	-	88	MHz	
	t_RSCK	Period	11.25	-	-	ns	
	RSCKH	High Period	5.625	-	-	ns	C_L=10pF
	RSCKL	Low Period	5.625	-	-	ns	C_L=10pF
		Duty cycle	-	50	-	%	
	RSTr/f	Rise/Fall Time	-	-	1.0	ns	
TCON_TSIG[11:0]	TSIGSU	Setup time	2.5	-	-	ns	C_L=10pF, SSWITCH[i]=0
	TSIGHD	Hold time	2.5	-	-	ns	C_L=10pF, SSWITCH[i]=0
TTL operation mode							
DISP0R[7:0], DISP0G[7:0], DISP0B[7:0]	DISPSU	Setup time	2.5	-	-	ns	C_L=10pF, Delay[i]=0
	DISPHD	Hold time	2.5	-	-	ns	C_L=10pF, Delay[i]=0
DISP0CLKO DISP0CLKOX	f_TTLCK	Frequency	-	-	88	MHz	
	t_TTLCK	Period	11.25	-	-	ns	
	TTLCKH	High Period	5.625	-	-	ns	C_L=10pF
	TTLCKL	Low Period	5.625	-	-	ns	C_L=10pF
		Duty cycle	-	50	-	%	
	t_rise/fall	Rise/Fall Time	-	-	1.0	ns	
TCON_TSIG[11:0]	TSIGSU	Setup time	2.5	-	-	ns	C_L=10pF, SSWITCH[i]=0
	TSIGHD	Hold time	2.5	-	-	ns	C_L=10pF, SSWITCH[i]=0
In Duty cycle is 50, Clock setting of Display0 should be frequency divided by even number. If clock setting of Display0 is frequency divided by odd number, duty cycle is not 50. Example: 1066/13= 82.05MHz. High period 7/13, low period 6/13 →53.8%. Example: 800/9= 88.88MHz. High period 5/9→55.6%, low period 4/9→44.4%.							

Table 2.34. : Max. frequency of DISP0 output cells in TTL mode

Drive strength	External lumped load (pf)			
	10	20	30	Unit
2mA	50	20	30	MHz
4mA	80	50	30	MHz
8mA	88	88	70	MHz

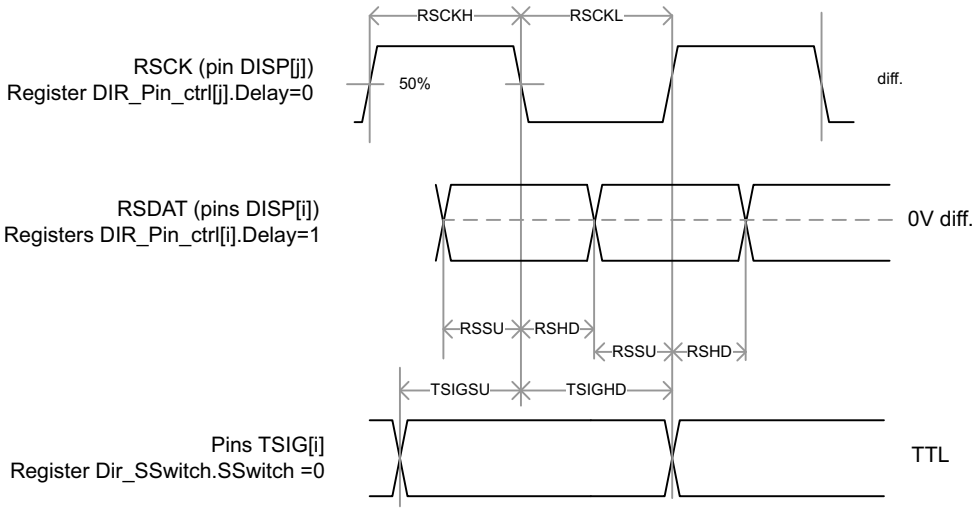


Figure 2.25. : RSDS operation output timing

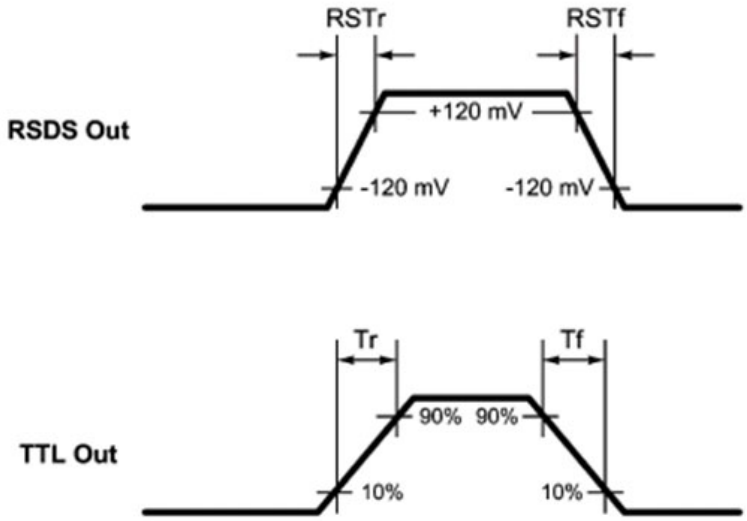


Figure 2.26. : RSDS/TTL operation output timing

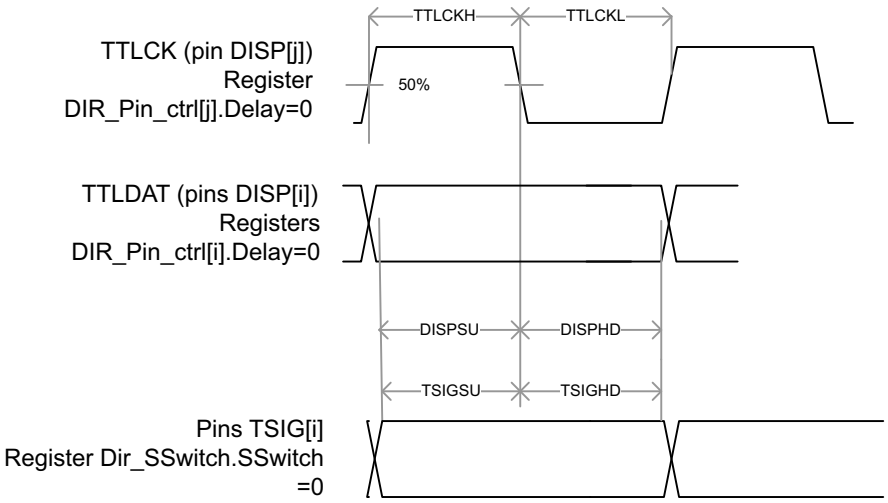


Figure 2.27. : TTL operation output timing (1)

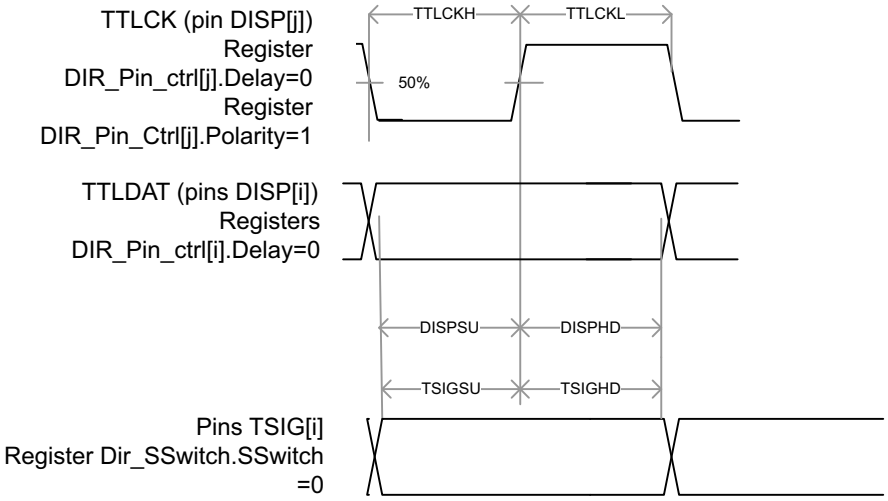


Figure 2.28. : TTL operation output timing (2)

2.5.3.5. ITU-R BT656 Display Timing DISP1 Interface

Table 2.35. : AC timing of ITU-R BT656 Display

Signal	Symbol	Description	Value			Unit
			Min	Typ	Max	
DISP1CLK	f_{DCLK}	Display1 clock frequency	-	-	27	MHz
	t_{DCLKH}	Display1 clock H width	17.4	-	-	ns
	t_{DCLKL}	Display1 clock L width	17.1	-	-	ns
DISP1VI[7:0]	t_{DVS}	Output Data setup time	10	-	-	ns
	t_{DVH}	Output Data hold Time	10	-	-	ns

MB86R11F: Method of making DISP1CLK= 27MHz

For example, if PLL output is 800MHz.

Frequency is divided with Display1. 800MHz/29 = 27.6MHz(f_{DCLK})

The divider 29 is an odd number, because duty is not 50.

High period 14/29 → 48.3%, low period 15/29 → 51.7%

Example: If DISP1CLK output is just 27MHz. The output of PLL should be made multiplication of 27MHz, and frequency is divided with Display1.

MB86R12/13: Method of making DISP1CLK= 27MHz

For example, if PLL output is 1066MHz.

Frequency is divided with Display1. 1066MHz/39 = 27.36MHz(f_{DCLK})

The divider 39 is an odd number, because duty is not 50.

High period 19/39 → 48.7%, low period 20/39 → 51.3%

Example: If DISP1CLK output is just 27MHz. The output of PLL should be made multiplication of 27MHz, and frequency is divided with Display1.

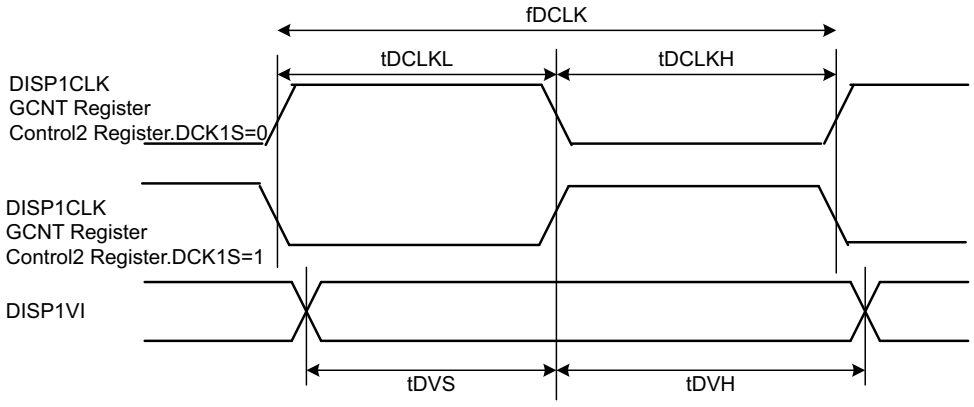


Figure 2.29. : ITU-R BT656 Display Timing

2.5.4. Video Capture Unit Signal Timing

2.5.4.1. Clock

Table 2.36. : AC timing of video capture interface clock signal

Signal	Symbol	Description	Value			Unit
			Min	Typ	Max	
CAP*n*CLK	f_{CCLK}	Capture clock frequency	-	-	133	MHz
	t_{HCCLK}	Capture clock H width	3	-	-	ns
	t_{LCCLK}	Capture clock L width	3	-	-	ns
Note: It depends on the resolution of the video capture.						

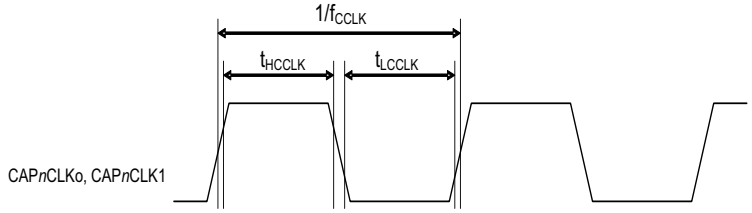


Figure 2.30. : Video capture clock input signal timing

2.5.4.2. Input Signal

Table 2.37. : AC timing of video capture interface input signal

Signal	Symbol	Description	Value			Unit
			Min	Typ	Max	
CAP*n*VI[7:0]	t_{SCVI}	Input setup time	6	-	-	ns
	t_{HCVI}	Input hold Time	1	-	-	ns
CAP0R [7:2]	t_{SCR}	Input setup time	6	-	-	ns
	t_{HCR}	Input hold Time	1	-	-	ns
CAP0G [7:2]	t_{SCG}	Input setup time	6	-	-	ns
	t_{HCG}	Input hold Time	1	-	-	ns
CAP0B [7:2]	t_{SCB}	Input setup time	6	-	-	ns
	t_{HCB}	Input hold Time	1	-	-	ns
CAP0HS	t_{SCHS}	Input setup time	6	-	-	ns
	t_{HCHS}	Input hold Time	1	-	-	ns
CAP0VS	t_{SCVS}	Input setup time	6	-	-	ns
	t_{HCVS}	Input hold Time	1	-	-	ns
CAP0FID	t_{SCF}	Input setup time	6	-	-	ns
	t_{HCF}	Input hold Time	1	-	-	ns
CAP0VAL	t_{SCV}	Input setup time	6	-	-	ns
	t_{HCV}	Input hold Time	1	-	-	ns

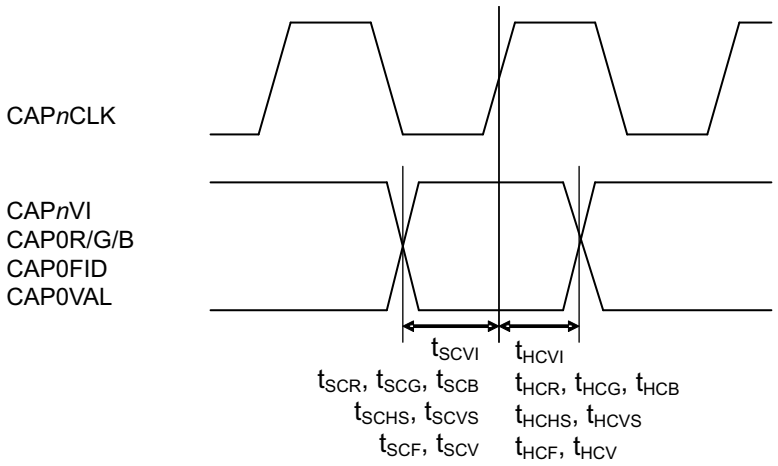


Figure 2.31. : Video capture input signal timing

2.5.5. I2S Signal Timing

Table 2.38. : AC timing of master mode (I2S)

Signal	Symbol	Description	Value			Unit
			Min	Typ	Max	
I2Sx_SCK (output)	t_{mcyc}	Operating frequency, I2Sx_SCK	–	–	T/CKRT	MHz
	t_{mhw}	Pulse duration, I2Sx_SCK high	0.45*T	–	0.55*T	ns
	t_{mlw}	Pulse duration, I2Sx_SCK low	0.45*T	–	0.55*T	ns
I2Sx_WS (output)	t_{dfs}	Delay time, I2Sx_SCK High to I2Sx_WS transition	0	–	12.0	ns
I2Sx_SDO	t_{ddo}	Delay time, I2Sx_SCK High to I2Sx_SDO valid except the first bit of transmit frame.	0	–	12.0	ns
	t_{dhz}	Delay time, I2Sx_SCK High to I2Sx_SDO HiZ time.	0	–	12.0	ns
I2Sx_SDI	t_{sdi}	Setup time, I2Sx_SDI valid before I2Sx_SCK Low	MB86R11F 11.0			
			MB86R12/13 9.0	–	–	ns
	t_{hdi}	Hold time, I2Sx_SDI valid after I2Sx_SCK Low	0	–	–	ns

T: T indicates the cycle of AHBCLK of the internal clock.
S: S indicates the cycle of I2Sx_SCK.
I2Sx_SDO/I2Sx_ WS is a delay value in CL=20pF.
CKRT: output clock frequency dividing. The internal clock mode prohibits setting CKRT to 0x00 and 0x01

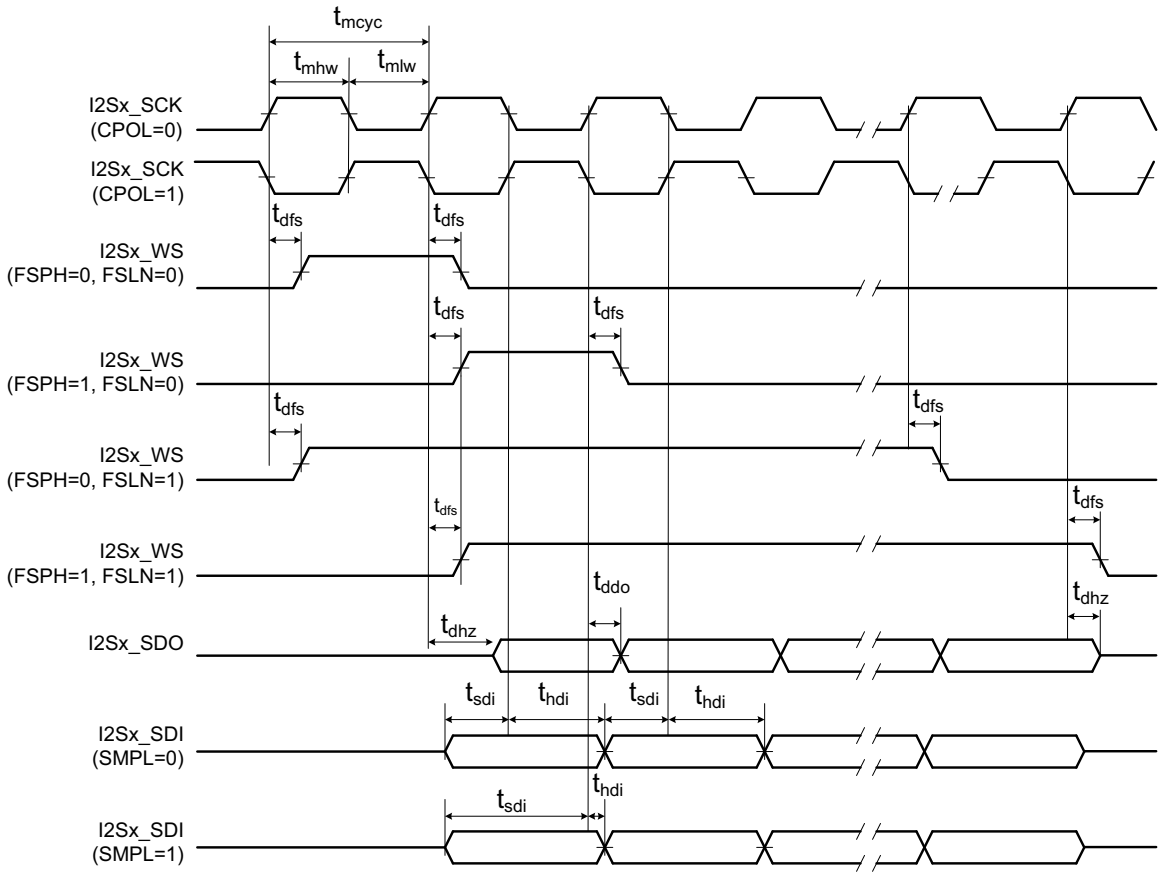


Figure 2.32. : Master Mode Timings (I2S)

Table 2.39. : AC timing of master mode (AC'97)

Signal	Symbol	Description	Value			Unit
			Min	Typ	Max	
I2Sx_ECLK	t_{ecyc}	Operating frequency, I2Sx_ECLK	–	–	24.576	MHz
	t_{ehw}	Pulse duration, I2Sx_ECLK high	0.45*E	–	0.55*E	ns
	t_{elw}	Pulse duration, I2Sx_ECLK low	0.45*E	–	0.55*E	ns
I2Sx_WS (output)	t_{efs}	Delay time, I2Sx_ECLK High to I2Sx_WS transition	0	–	16.0	ns
I2Sx_SDO	t_{edo}	Delay time, I2Sx_ECLK High to I2Sx_SDO valid except the first bit of transmit frame.	0	–	16.0	ns
	t_{ehz}	Delay time, I2Sx_SCK High to I2Sx_SDO HiZ time.	0	–	16.0	ns
I2Sx_SDI	t_{esdi}	Setup time, I2Sx_SDI valid before I2Sx_ECLK Low	4.0	–	–	ns
	t_{ehdi}	Hold time, I2Sx_SDI valid after I2Sx_ECLK Low	0	–	–	ns
E: The I2Sx_ECLK cycle is indicated. I2Sx_SDO/I2Sx_ WS is a delay value in CL=20pF.						

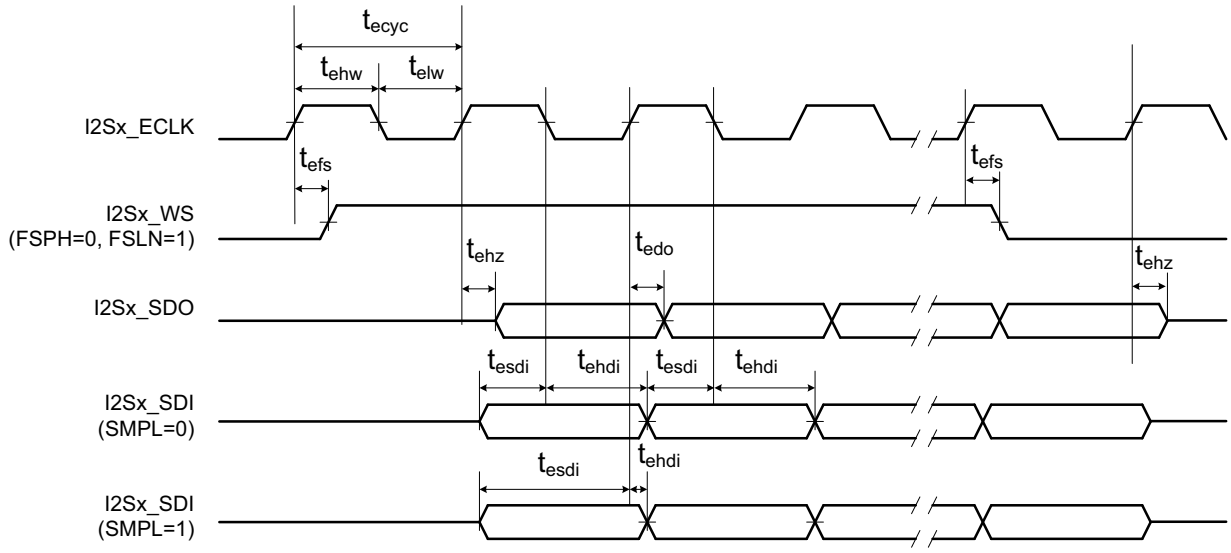


Figure 2.33. : Master Mode Timings(AC'97)

Table 2.40. : AC timing of slave mode (I2S)

Signal	Symbol	Description	Value			Unit
			Min	Typ	Max	
I2Sx_SCK (input)	t_{scyc}	Operating frequency, I2Sx_SCK	–	–	24.576	MHz
	t_{shw}	Pulse duration, I2Sx_SCK High	0.45*T	–	0.55*T	ns
	t_{slw}	Pulse duration, I2Sx_SCK Low	0.45*T	–	0.55*T	ns
I2Sx_WS (input)	t_{sfi}	Setup time, external I2Sx_WS High before I2Sx_SCK Low	MB86R11F: 4.0 MB86R12/13: 4.5	–	–	ns
	t_{hfi}	Hold time, external I2Sx_WS High after I2Sx_SCK Low	0	–	–	ns
I2Sx_SDO	t_{ddo}	Delay time, I2Sx_SCK high to I2Sx_SDO valid except the first bit of transmit frame.	0	–	16.0	ns
	t_{dhz}	Delay time, I2Sx_SCK High to I2Sx_SDO HiZ time.	0	–	16.0	ns
	t_{dfb1}	Delay time, I2Sx_SCK high to the first bit of a transmit frame when FSPH bit of I2Sx_CNTREG register is 1.	0	–	16.0	ns
I2Sx_SDI	t_{sdi}	Setup time, I2Sx_SDI valid before I2Sx_SCK Low	4.0	–	–	ns
	t_{hdi}	Hold time, I2Sx_SDI valid after I2Sx_SCK Low	0	–	–	ns

T: The I2Sx_SCK cycle is indicated.
I2Sx_SDO is a delay value in CL=20pF.

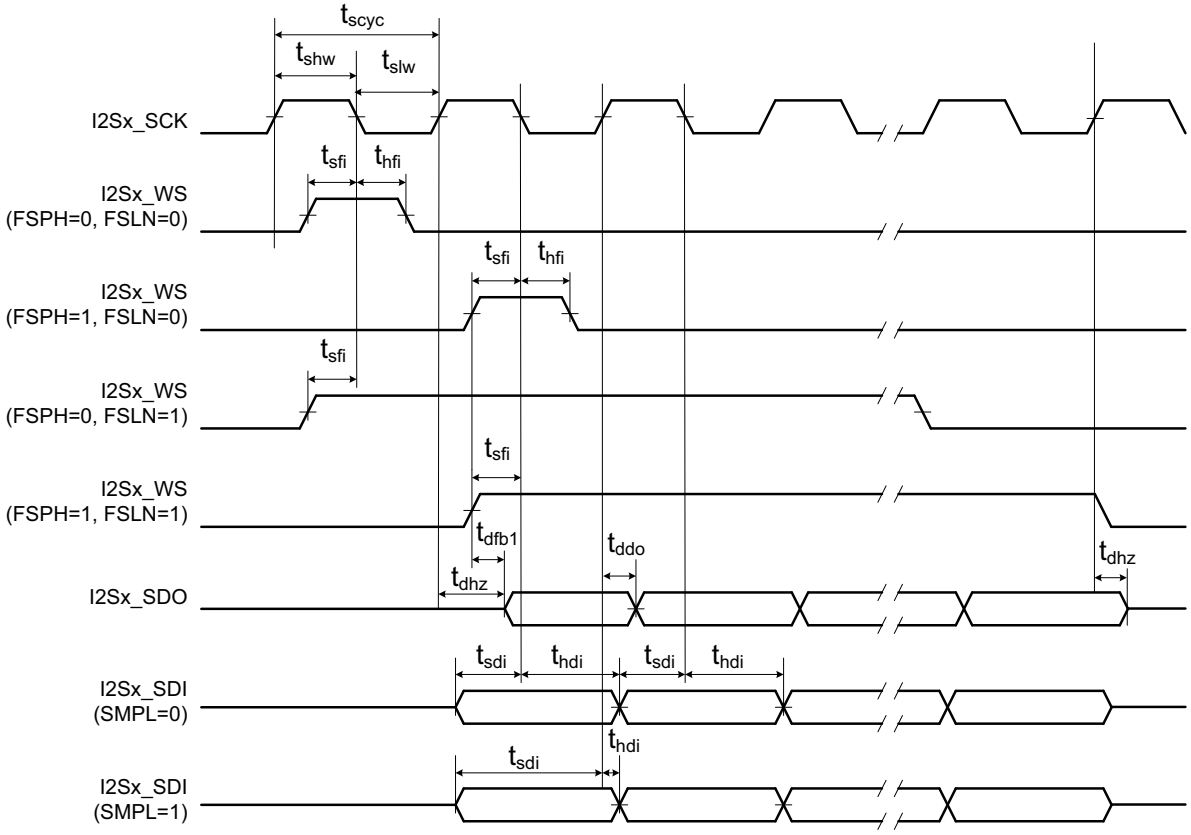


Figure 2.34. : Slave Mode Timings

2.5.6. UART Signal Timing

Table 2.41. : AC timing

Signal	Symbol	Description	Value			Unit
			Min	Typ	Max	
UART0_SIN UART1_SIN UART2_SIN UART3_SIN UART4_SIN UART5_SIN	t_{dw}	Input data width	16*A	-	-	ns
UART*_XCTS (*:0-3)	t_{ctsw}	Input XCTS data width	A	-	-	ns
UART*_SIN are connected to USART*_SIN pins(*:0-5). A is a cycle of the internal APBCLK.						

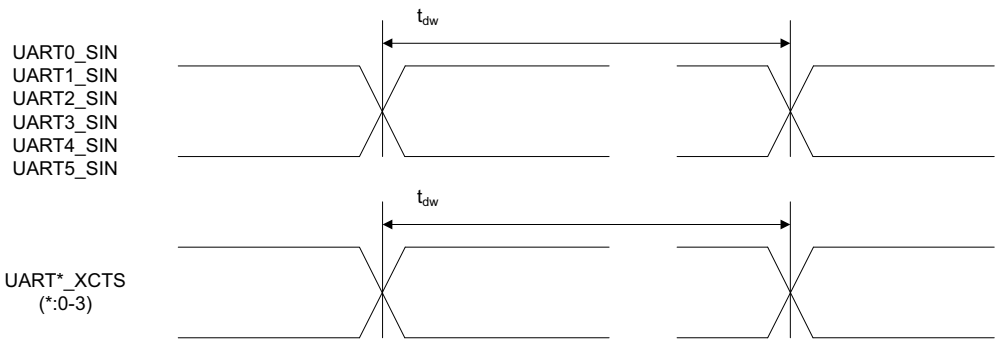


Figure 2.35. : UART timing

2.5.7. I2C Bus Timing

It is strongly recommended to use the I2C0 pin 1.

Limitation: Because some I/O pins cannot be used exclusively, the I2C standard values for Tr/Tf(min) in high-speed mode cannot be realized for pins I2C[4:2].

Table 2.42. : AC timing of I2C signal

Signal	Symbol	Description		Value			Unit
				Min	Typ	Max	
I2Cx_SDA	T_{S2SDAI}	SDAI setup time	Normal mode	250 [1)]	-	-	ns
			High-speed mode	100 [1)]	-	-	ns
	T_{H2SDAI}	SDAI hold time	Normal mode	0.0 [1)]	-	-	ns
			High-speed mode	0.0 [1)]	-	-	ns
	T_{WBFI}	BUS free time	Normal mode	4.7 [1)]	-	-	µs
			High-speed mode	1.3 [1)]	-	-	µs
	T_{H2SDAO}	SDAO hold time		5	-	-	PCLK [3)]
I2Cx_SCL	T_{CSCLI}	SCLI cycle time	Normal mode	10.0 [1)]	-	-	µs
			High-speed mode	2.5 [1)]	-	-	µs
	T_{WHSCLI}	SCLI H width	Normal mode	4.0 [1)]	-	-	µs
			High-speed mode	0.6 [1)]	-	-	µs
	T_{WLSCLI}	SCLI L width	Normal mode	4.7 [1)]	-	-	µs
			High-speed mode	1.3 [1)]	-	-	µs
	T_{CSCLO}	SCLO cycle time	Normal mode	2*m + 2 [2)]	-	-	PCLK [3)]
			High-speed mode	Int (1.5*m) + 2 [2)]	-	-	PCLK [3)]
	T_{WHSCLO}	SCLO H width	Normal mode	m + 2 [2)]	-	-	PCLK [3)]
			High-speed mode	Int (0.5*m) + 2 [2)]	-	-	PCLK [3)]
	T_{WLSCLO}	SCLO L width	Normal mode	m [2)]	-	-	PCLK [3)]
			High-speed mode	m [2)]	-	-	PCLK [3)]
	T_{S2SCLI}	SCLI setup time	Normal mode	4.7 [2)]	-	-	µs
			High-speed mode	0.6 [2)]	-	-	µs
	T_{H2SCLI}	SCLI hold time	Normal mode	4.0 [2)]	-	-	µs
			High-speed mode	0.6 [2)]	-	-	µs
	T_{S2SCLO}	SCLO setup time	Normal mode	m+2 [2)]	-	-	PCLK [3)]
			High-speed mode	Int(0.5*m) + 2 [2)]	-	-	PCLK [3)]
	T_{H2SCLO}	SCLKO hold time	Normal mode	m – 3 [2)]	-	-	PCLK [3)]
				CS-(2*FS+1) [4)]	-	-	PCLK [3)]
			High-speed mode	Int(0.5*m) – 3 [2)]	-	-	PCLK [3)]
				Int(0.5*CS) – (2*FS+1) [4)]	-	-	PCLK [3)]

Table 2.42. : AC timing of I2C signal

Signal	Symbol	Description		Value			Unit
				Min	Typ	Max	
SCL/SDA	Tr	SCL risetime	Normal mode	-	-	5% of SCK[6)] 1000	ns
			High-speed mode	20 + 0.1Cb[5)]	-	5% of SCK[6)] 300	ns
	Tf	SCL falltime	Normal mode	-	-	5% of SCK[6)] 300	ns
			High-speed mode	20 + 0.1Cb[5)]	-	5% of SCK[6)] 300	ns

1) I^2C bus standard value.

2) "m" value is a register setting value. See Clock Control register (I2CxCCR) in the I2C interface for more details.

3) PCLK = APBCLK cycle.

4) When you use Expand Clock period select register (I2CxCSR) and I2C System Clock Frequency select register (I2CxFSR)

5) C_b=Total capacity of one bus line.(pF)

6) Max value for MB86R11F

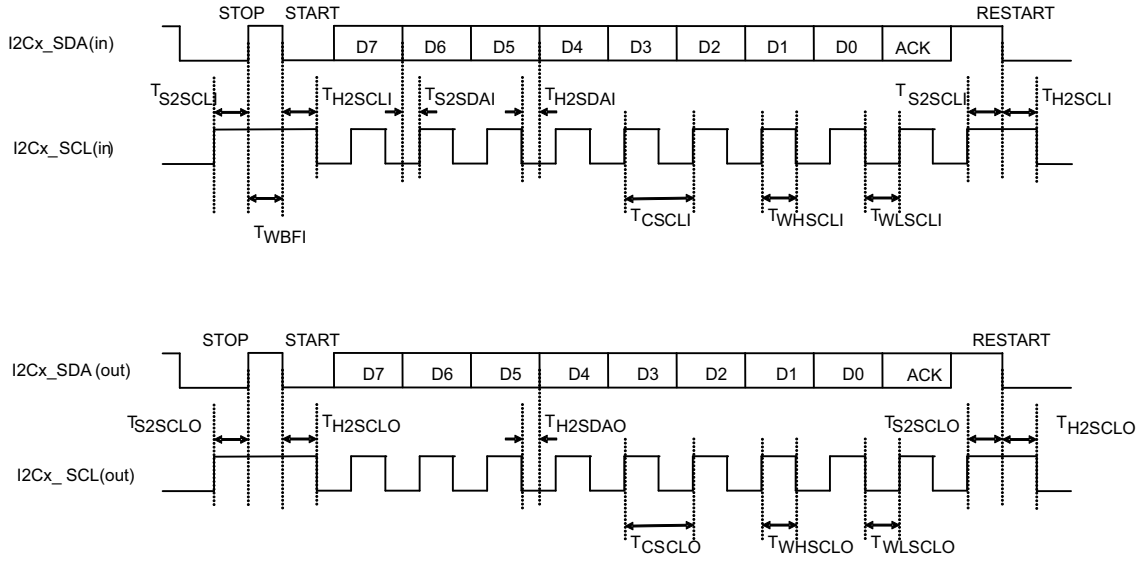


Figure 2.36. : I2C access timing

2.5.8. SFI Signal Timing

Table 2.43. : SFI AC timing

Signal	Symbol	Description	Value			Unit
			Min	Typ	Max	
SPIx_SCK	t_{cyc}	Operating frequency	-	-	MB86R11F: 0.5*A MB86R12/13: 0.5*B	MHz
SPIx_DI	t_{sdi}	Setup time, SPIx_DI valid before SPIx_SCK	7	-	-	ns
	t_{hdi}	Hold time, SPIx_DI valid after SPIx_SCK	0	-	-	ns
SPIx_DO	t_{do}	Delay time, SPIx_SCK	-2	-	3	ns
SPIx_SS	t_{sso}	Delay time, SPIx_SCK	-2	-	3	ns

A: The AHBCLK frequency.
B: The APBCLK frequency.

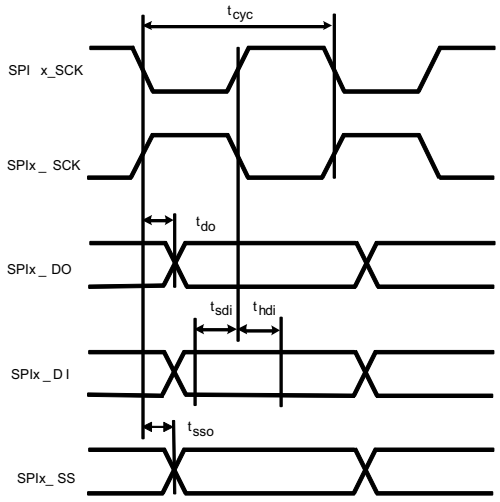


Figure 2.37. : SFI timing

The polarity of SPIx_SCK is decided by the register setting.

2.5.9. CAN Signal Timing

Table 2.44. : CAN AC timing

Signal	Symbol	Description	Value			Unit
			Min	Typ	Max	
CAN0_TX CAN1_TX	t_{do}	Data output delay time	-	-	17	ns
CAN0_RX CAN1_RX	t_{dw}	Input data width	1000	-	-	ns

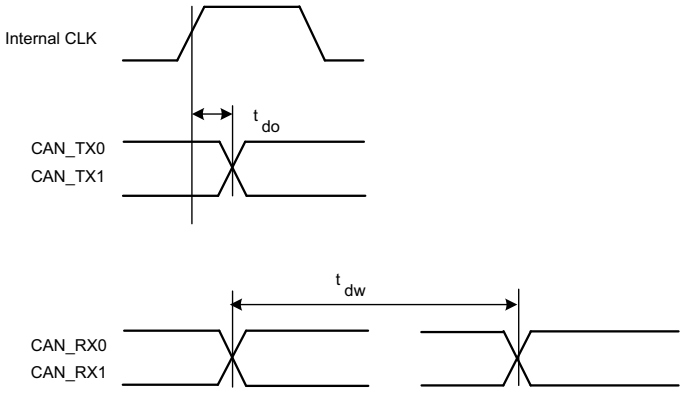


Figure 2.38. : CAN timing

2.5.10. MediaLB Signal Timing

2.5.10.1. MediaLB AC Spec Type A

Ground = 0V; Load capacitance = 60pF; MediaLB speed = 256Fs or 512Fs; Fs = 48kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

2.5.10.1.1. Clock

Table 2.45. : AC Timing of Clock Signal

Signal	Symbol	Description	Value			Unit	Signal
			Min	Typ	Max		
MLB_CLK	f_{mck}	MLB_CLK operating frequency[1)]	11.264 - -	- 22.5792 -	- - 24.6272	MHz	256xFs at 44.0kHz 512xFs at 44.1kHz 512xFs at 48.1kHz
	t_{mckr}	MLB_CLK rising time	-	-	3	ns	V_{IL} to V_{IH}
	t_{mckf}	MLB_CLK falling time	-	-	3	ns	V_{IH} to V_{IL}
	t_{mckc}	MLB_CLK cycle time	- -	81 40	- -	ns	256xFs 512xFs
	t_{mckl}	MLB_CLK low time	31.5 14.5	37 17	- -	ns	256xFs 512xFs
	t_{mckh}	MLB_CLK high time	31.5 14.4	38 17	- -	ns	256xFs 512xFs
	t_{mpwv}	MLB_CLK pulse width variation	-	-	2	ns pp	2)

1): The controller can shut Off MLB_CLK to place MediaLB in a low-power state.
2): Pulse width variation is measured at 1.25V by triggering on one edge of MLB_CLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp).

2.5.10.1.2. Input Signal

Table 2.46. : AC Timing of Input Signal

Signal	Symbol	Description	Value			Unit	Comment
			Min	Typ	Max		
MLB_SIG, MLB_DAT input	t_{dsmcf}	MLB_SIG and MLB_DAT input valid to MLB_CLK falling	1	-	-	ns	
	t_{dhmcf}	MLB_SIG and MLB_DAT input hold from MLB_CLK low	0	-	-	ns	

2.5.10.1.3. Output Signal

Table 2.47. : AC Timing of Output Signal

Signal	Symbol	Description	Value			Unit	Comment
			Min	Typ	Max		
MLB_SIG, MLB_DAT output	t_{mcfdz}	MLB_SIG and MLB_DAT output high impedance from MLB_CLK low	0	-	t_{mckl}	ns	
	t_{mdzh}	Bus hold time	4	-	-	ns	1)

1): The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

2.5.10.2. MediaLB AC Spec Type B

GND = 0V; Load capacitance = 40pF; MediaLB speed = 1024Fs; Fs = 48kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

2.5.10.2.1. Clock

Table 2.48. : AC Timing of Clock Signal

Signal	Symbol	Description		Value			Unit	Comment
				Min	Typ	Max		
MLB_CLK	f_{mck}	MLB_CLK operating frequency 1)		45.056 - -	- 49.152 -	- - 49.254	MHz	1024xFs at 44.0kHz 1024xFs at 48.0kHz 1024xFs at 48.1kHz
	t_{mckr}	MLB_CLK rising time		-	-	1	ns	V_{IL} to V_{IH}
	t_{mckf}	MLB_CLK falling time		-	-	1	ns	V_{IH} to V_{IL}
	t_{mckc}	MLB_CLK cycle time		-	20.3	-	ns	
	t_{mckl}	MLB_CLK low time	MB86R11F	6.5	7.7	-	ns	
			MB86R12/13	6.8	7.8			
	t_{mckh}	MLB_CLK high time	MB86R11F	9.7	10.6	-	ns	
			MB86R12/13	9.7	10.4			
	t_{mpwv}	MLB_CLK pulse width variation		-	-	0.5	ns pp	2)

1): The controller can shut Off MLB_CLK to place MediaLB in a low-power state.
2): Pulse width variation is measured at 1.25V by triggering on one edge of MLB_CLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp).

2.5.10.2.2. Input Signal

Table 2.49. : AC Timing of Input Signal

Signal	Symbol	Description	Value			Unit	Comment
			Min	Typ	Max		
MLB_SIG, MLB_DAT input	t_{dsmcf}	MLB_SIG and MLB_DAT input valid to MLB_CLK falling	1	-	-	ns	
	t_{dhmcf}	MLB_SIG and MLB_DAT input hold from MLB_CLK low	0	-	-	ns	

2.5.10.2.3. Output Signal

Table 2.50. : AC Timing of Output Signal

Signal	Symbol	Description	Value			Unit	Comment
			Min	Typ	Max		
MLB_SIG, MLB_DAT output	t_{mcfdz}	MLB_SIG and MLB_DAT output high impedance from MLB_CLK low	0	-	t_{mckl}	ns	
	t_{mdzh}	Bus hold time	2	-	-	ns	1)
1): The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.							

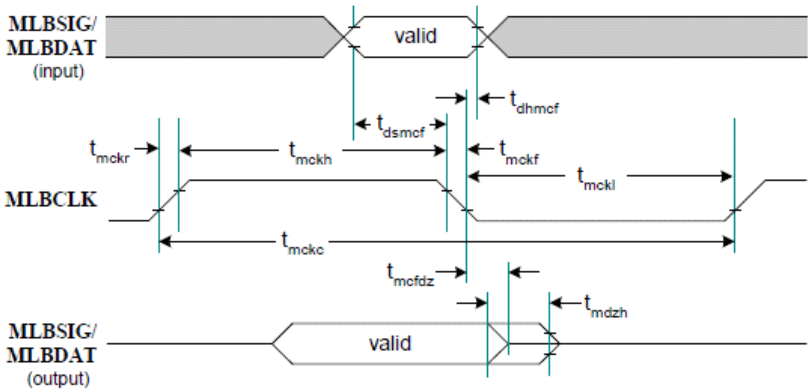


Figure 2.39. : MediaLB timing

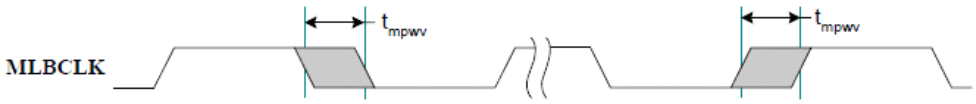


Figure 2.40. : MediaLB pulse width change timing

2.5.11. USB Signal Timing - MB86R11F

Table 2.51. : High-speed AC timing

Signal	Symbol	Description	Value			Unit
			Min	Typ	Max	
USBx_DP USBx_DM	Driver characteristics:					
	t_{hsr}	Rise time (10 - 90%)	500	-	-	ps
	t_{hsf}	Fall time (10 - 90%)	500	-	-	ps
	-	Driver waveform requirements	MB86R11F: Complies with USB2.0 specification			
	zhsdrv	Driver output resistance (also serves as high-speed termination)	40.5	-	49.5	-
	Clock timing:					
	thsdrat	High-speed data rate	479.760	-	480.240	Mb/s
	High-speed data timing					
	-	Data source jitter	MB86R11F: Complies with USB2.0 specification			
	-	Receiver jitter tolerance				

Table 2.52. : Full-speed AC timing

Signal	Symbol	Description	Value			Unit
			Min	Typ	Max	
USBx_DP USBx_DM	Driver characteristics:					
	t_{fr}	Rise time (10 - 90%)	4	-	20	ns
	t_{ff}	Fall time (10 - 90%)	4	-	20	ns
	t_{frfm}	Difference rise and fall time matching	90	-	111.11	%
	Clock timing: (in case of using UTM i/f and setting FSSEL="0")					
	tfdraths	Full-speed data rate for hubs and devices which are capable of high speed	11.9940	-	12.0060	Mb/s
	Full-speed data timings: (in case of using UTMI i/f and setting FSSEL="0")					
	t_{dj1} t_{dj2}	Source jitter total (including freq. tolerance): To next transition For paired transitions	 -3.5 -4	 - -	 3.5 4	ns
	t_{fdeop}	Source jitter for differential transition to SE0 transition	-2	-	5	ns
	t_{jr1} t_{jr2}	Receiver jitter: For next transition For paired transitions	 -18.5 -9	 -	 18.5 9	ns
	t_{feopt}	Source SE0 interval of EOP	160	-	175	ns
	t_{feopr}	Receiver SE0 interval of EOP	82	-	-	ns
	t_{fst}	Width of SE0 interval during differential transition	-	-	14	ns

Table 2.53. : Low-speed AC timing

Signal	Symbol	Description	Value			Unit
			Min	Typ	Max	
USBx_DP USBx_DM	Driver characteristics:					
	t_{lr}	Rise time (10 - 90%)	75	-	300	ns
	t_{lf}	Fall time (10 - 90%)	75	-	300	ns
	t_{lrfm}	Rise and fall time matching	80	-	125	%

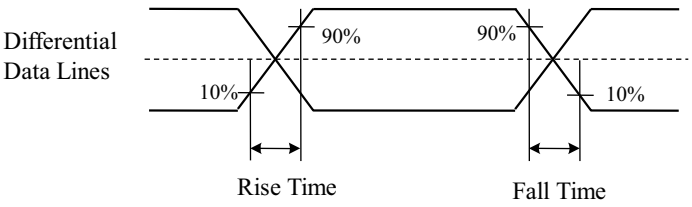


Figure 2.41. : Data signal fall and rise time

2.5.12. IDE66 Signal Timing

2.5.12.1. IDE PIO Timing

Table 2.54. : AC timing of register access

Symbol	Description	Value					Unit
		Mode0	Mode1	Mode2	Mode3	Mode4	
t_0	Cycle time (min.)	600	383	330	180	120	ns
t_1	Address valid to IDE_XDIOR/IDE_XDIOW setup (min.)	70	50	30	30	25	ns
t_2	IDE_XDIOR/IDE_XDIOW pulse width 8 bit (min.)	290	290	290	80	70	ns
t_{2i}	IDE_XDIOR/IDE_XDIOW recovery time (min.)	-	-	-	70	25	ns
t_3	IDE_XDIOW data setup (min.)	60	45	30	30	20	ns
t_4	IDE_XDIOW data hold (min.)	30	20	15	10	10	ns
t_5	IDE_XDIOR data setup (min.)	50	35	20	20	20	ns
t_6	IDE_XDIOR data hold (min.)	5	5	5	5	5	ns
t_{6Z}	IDE_XDIOR data tristate (max.)	30	30	30	30	30	ns
t_9	IDE_XDIOR/IDE_XDIOW to address valid hold (min.)	20	15	10	10	10	ns
t_{RD}	Read data valid to IDE_DIORDY active (if IDE_DIORDY initially low after tA) (min.)	0	0	0	0	0	ns
t_A	IDE_DIORDY setup time	35	35	35	35	35	ns
t_B	IDE_DIORDY pulse width (max.)	1250	1250	1250	1250	1250	ns
t_C	IDE_DIORDY assertion to release (max.)	5	5	5	5	5	ns

Table 2.55. : AC timing of data access

Symbol	Description	Value					Unit
		Mode0	Mode1	Mode2	Mode3	Mode4	
t_0	Cycle time (min.)	600	383	240	180	120	ns
t_1	Address valid to IDE_XDIOR/IDE_XDIOW setup (min.)	70	50	30	30	25	ns
t_2	IDE_XDIOR/IDE_XDIOW pulse width 8 bit (min.)	165	125	100	80	70	ns
t_{2i}	IDE_XDIOR/IDE_XDIOW recovery time (min.)	-	-	-	70	25	ns
t_3	IDE_XDIOW data setup (min.)	60	45	30	30	20	ns
t_4	IDE_XDIOW data hold (min.)	30	20	15	10	10	ns
t_5	IDE_XDIOR data setup (min.)	50	35	20	20	20	ns
t_6	IDE_XDIOR data hold (min.)	5	5	5	5	5	ns
t_{6Z}	IDE_XDIOR data tristate (max.)	30	30	30	30	30	ns
t_9	IDE_XDIOR/IDE_XDIOW to address valid hold (min.)	20	15	10	10	10	ns
t_{RD}	Read data valid to IDE_DIORDY active (if IDE_DIORDY initially low after tA) (min.)	0	0	0	0	0	ns
t_A	IDE_DIORDY setup time	35	35	35	35	35	ns
t_B	IDE_DIORDY pulse width (max.)	1250	1250	1250	1250	1250	ns
t_C	IDE_DIORDY assertion to release (max.)	5	5	5	5	5	ns

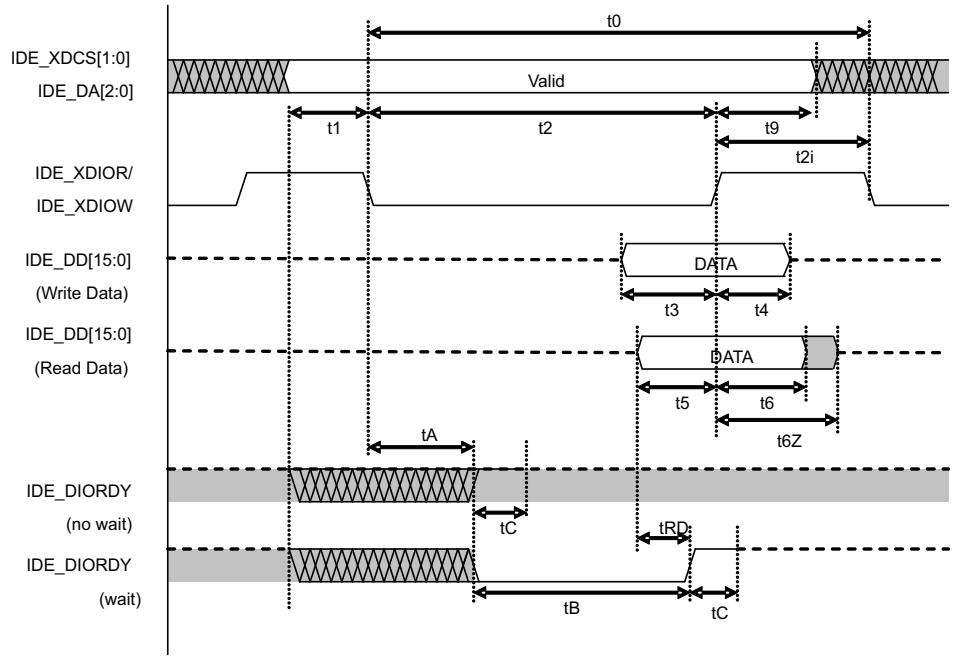


Figure 2.42. : PIO access timing

2.5.12.2. IDE Ultra DMA Timing

Table 2.56. : AC timing of Ultra DMA

Symbol	Description	Value										Unit
		mode0		mode1		mode2		mode3		mode4		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$T_{2cycleTYP}$	Typical sustained average 2 cycle time	240	-	160	-	120	-	90	-	60	-	ns
T_{2cycle}	2 cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	230	-	154	-	115	-	86	-	57	-	ns
T_{cycle}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	112	-	73	-	54	-	39	-	25	-	ns
T_{dvs}	Data valid setup time at sender (from data valid until STROBE edge)	70	-	48	-	30	-	20	-	6.7	-	ns
T_{dvh}	Data valid setup time at sender (from STROBE edge until data may become invalid)	6.2	-	6.2	-	6.2	-	6.2	-	6.2	-	ns
T_{fs}	First STROBE time (for device to first negate DSTROBE from STOP during data in Burst)	-	230	-	200	-	170	-	130	-	120	ns
T_{li}	Limited interlock time	0	150	0	150	0	150	0	100	0	100	ns
T_{mli}	Interlock time with minimum	20	-	20	-	20	-	20	-	20	-	ns
T_{ui}	Unlimited interlock time	0	-	0	-	0	-	0	-	0	-	ns
T_{az}	Maximum time allowed for output drivers to release (from asserted or negated)	-	10	-	10	-	10	-	10	-	10	ns
T_{zah}	Minimum delay time required for output	20	-	20	-	20	-	20	-	20	-	ns
T_{zad}	Drivers to assert or negate (from released)	0	-	0	-	0	-	0	-	0	-	ns
T_{env}	Envelope time (from DMACK- to STOP and HDMARDY- during data in burst initiation and from IDE_XDDDMACK to STOP during data out burst initiation)	20	70	20	70	20	70	20	55	20	55	ns
T_{rfs}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY)	-	75	-	70	-	60	-	60	-	60	ns
T_{rp}	Minimum time to assert STOP or negate IDE_DMARQ	160	-	125	-	100	-	100	-	100	-	ns
T_{iordyz}	Maximum time before releasing IDE_DIORDY	-	20	-	20	-	20	-	20	-	20	ns
t_{ziordy}	Minimum time before driving STROBE	0	-	0	-	0	-	0	-	0	-	ns

Table 2.56. : AC timing of Ultra DMA (Continued)

Symbol	Description	Value										Unit
		mode0		mode1		mode2		mode3		mode4		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T_{ack}	Setup and hold times for DMACK- (before assertion or negation)	20	-	20	-	20	-	20	-	20	-	ns
T_{ss}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates burst)	50	-	50	-	50	-	50	-	50	-	ns

Ultra DMA Read access

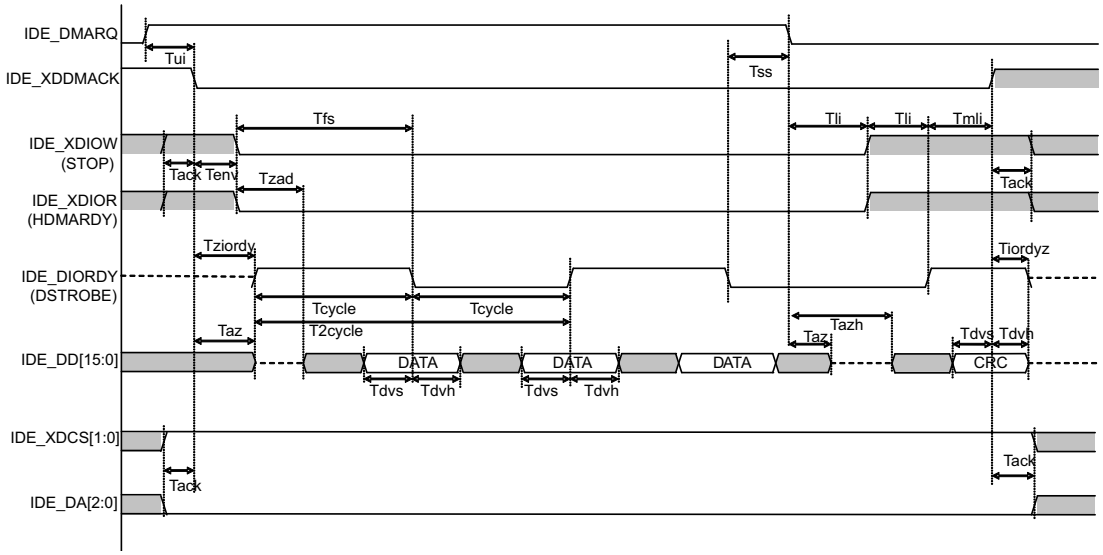


Figure 2.43. : IDE Read access timing

Ultra DMA Write access

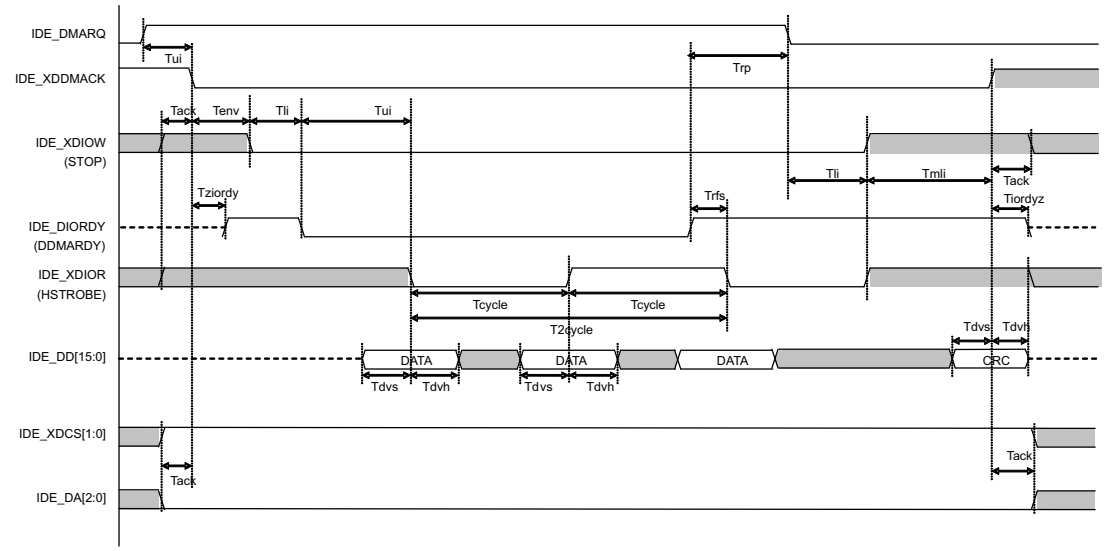


Figure 2.44. : IDE Write access timing

2.5.13. USART Signal Timing

At MB86R11F, MB86R12, MB86R13, these pin names in the table are corresponding to external pin names as follows.

SCKn: USARTn_SCK

SINn: USARTn_SIN

SOTn: USARTn_SOUT

(Vcc=3.3V, C_load=20pF)

Table 2.57. : USART AC timing

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal Shift Clock Mode	MB86R11F: 5 t_{CLKP1} MB86R12/13: 4 t_{CLKP1}	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKn SOTn		-10	+10	ns
SOT→SCK↑delay time	t_{OVSHI}	SCKn SOTn		MB86R11F: N * t_{CLKP1} -10 1) MB86R12/13: N * t_{CLKP1} -25 1)	-	ns
Valid SIN →SCK↑	t_{IVSHI}	SCKn SINn		MB86R11F: t_{CLKP1} +25 MB86R12/13: t_{CLKP1} +10	-	ns
SCK↑→Valid SIN hold time	t_{SHIXI}	SCKn SINn		0	-	ns
Serial clock “L”pulse width	t_{SLSHE}	SCKn	External Shift Clock Mode	t_{CLKP1}+10	-	ns
Serial clock “H”pulse width	t_{SHSLE}	SCKn		t_{CLKP1}+10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKn SOTn		-	$2t_{CLKP1}$+40	ns
Valid SIN →SCK↑	t_{IVSHE}	SCKn SINn		t_{CLKP1}/2+10	-	ns
SCK↑→Valid SIN hold time	t_{SHIXE}	SCKn SINn		t_{CLKP1}+10	-	ns
SCK fall time	t_{FE}	SCKn		-	5% of SCK	ns
SCK rise time	t_{RE}	SCKn		-	5% of SCK	ns

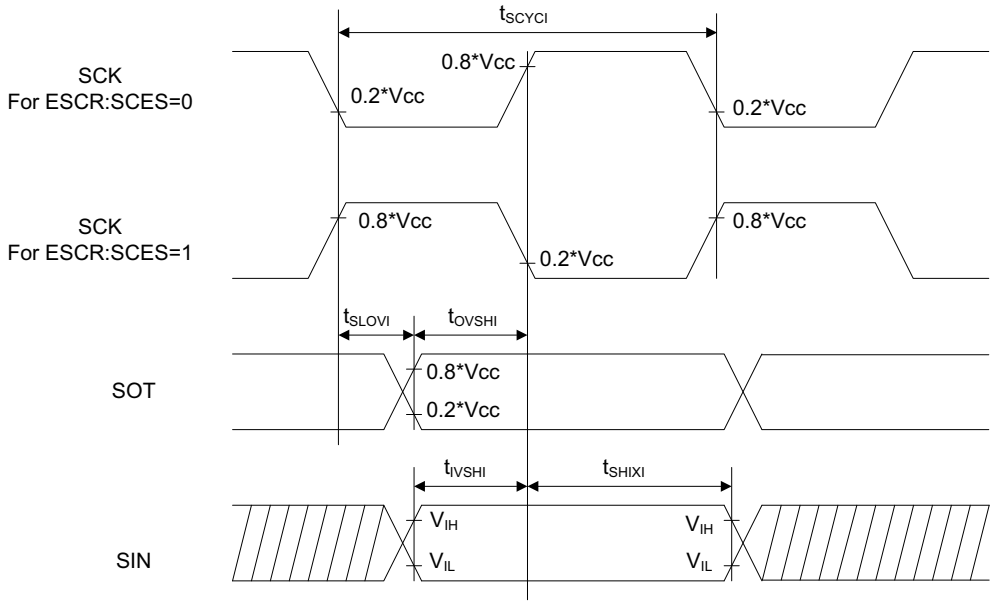
1): Parameter N depends on tSCYCI and can be calculated as follows:

if tSCYCI = 2*k*tCLKP1, then N = k, where k is an integer > 2

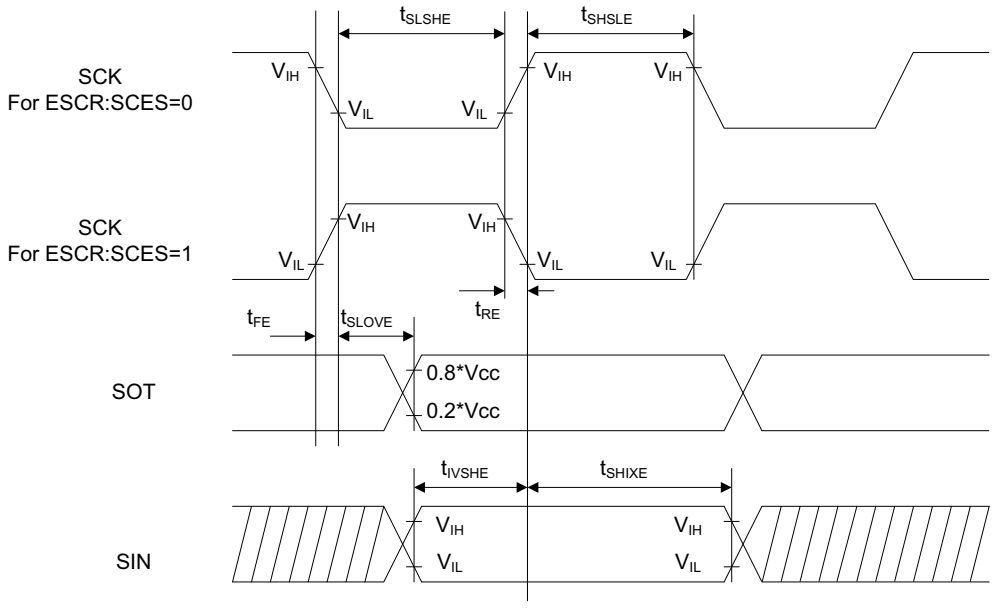
if tSCYCI = (2*k+1)*tCLKP1, then N = k+1, where k is an integer > 1

CLKP is APBCLK

These value is calculated at Input slew 1.5ns



Internal Shift Clock Mode



External Shift Clock Mode

Figure 2.45. : USART timing

2.5.14. Ethernet Signal Timing

2.5.14.1. MII Timing

(Vcc=3.3V Cload=20pF)

Table 2.58. : Ethernet AC timing of MII

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
RXD[3:0],RX_DV,RX_ER setup to RX_CLK high	t_{RSET}	10	-	-	ns
RXD[3:0],RX_DV,RX_ER hold RX_-CLK high	t_{SLOVI}	10	-	-	ns
TXD[3:0],TX_EN,TX_ER output delay	t_{Tdelay}	0	-	16	ns

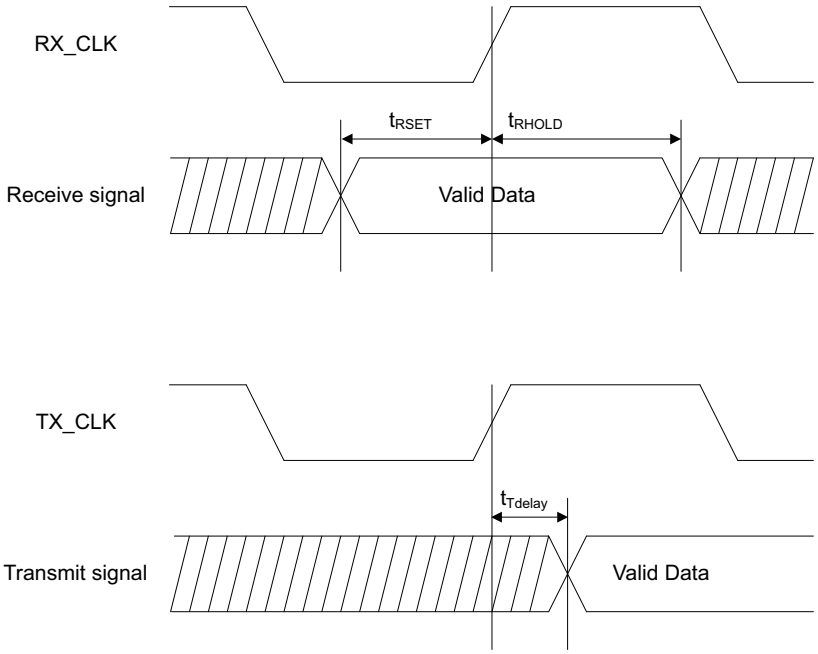


Figure 2.46. : MII timing

2.5.14.2. RMII Timing

Table 2.59. : Ethernet AC timing of RMII

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
RXD[1:0],RX_DV setup to OSC_-CLK high	t_{RSET_RM}	4	-	-	ns
RXD[1:0],RX_DV hold to OSC_CLK high	t_{RHOLD_RM}	2	-	-	ns
OSC_CLK high to transmit TXD[1:0],TX_EN valid	t_{TSET_RM}	4	-	-	ns
OSC_CLK high to transmit TXD[1:0],TX_EN not valid	t_{HOLD_RM}	2	-	-	
OSC_CLK frequency			50		MHz

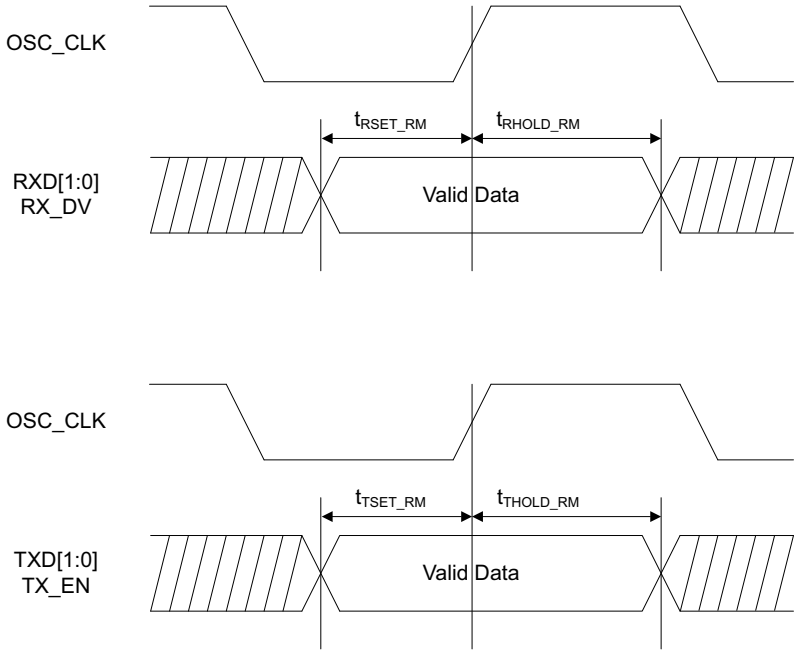


Figure 2.47. : RMII timing

2.5.14.3. MDIO Timing

(Vcc=3.3V Cload=20pF)

Table 2.60. : Ethernet AC MDIO if timing of MII

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
MDIO setup before MDC,sourced by STA	t_{MDISET}	-	MB86R11F: 15 MB86R12/13: 10	-	ns
MDIO hold after MDC, sourced by STA	$t_{MDIHOLD}$	-	10	-	ns
MDC to MDIO output delay,sourced by PHY	$t_{MDOdelay}$	-	-	50	ns
MDC period	MDCsycle	-	420	-	ns

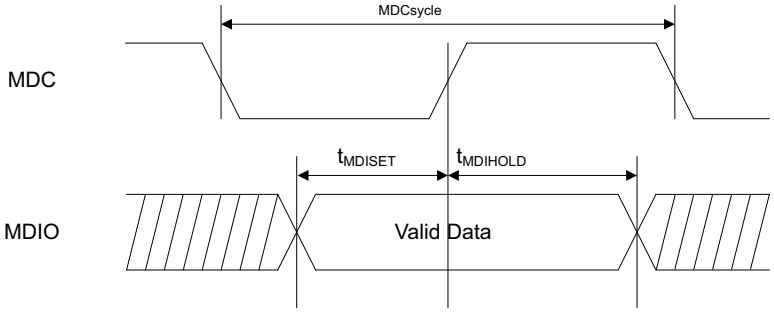


Figure 2.48. : MDIO input timing

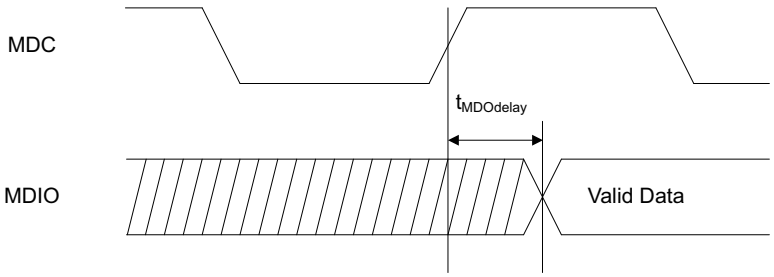


Figure 2.49. : MDIO output timing

2.5.15. TS Signal Timing

2.5.15.1. TS CLK Not Inverted Mode

Table 2.61. : TS AC timing of TS clock not inverted mode

Signal	Symbol	Description	Value			Unit
			Min	Typ	Max	
TS0CLK,TS1CLK (TS SCLK)	t_{scyc}	TS serial clock frequency	-	-	100	MHz
TS0CTL1, TS1CTL1, TS0CTL2, TS2CTL2 (TS SIN)	t_{sset}	Input signal setup time of serial mode	4	-	-	ns
	t_{shold}	Input signal hold time of serial mode	1	-	-	ns
TSCLK (TS PCLK)	t_{pcyc}	TS parallel clock frequency	-	-	AHB /6	MHz
TSDATA0,TSDATA1, TSDATA2, TSDATA3, TSDATA4, TSDATA5, TSDATA6, TSDATA7, TSCTL1, TSCTL2 (TS PIN)	t_{pset}	Input signal setup time of parallel mode	4	-	-	ns
	t_{phold}	Input signal hold time of parallel mode	1	-	-	ns
AHB : The AHB bus clock frequency is shown.						

At TsClk bit of TSD_INPUT_CFG register is 0, TS signal timing becomes the following.

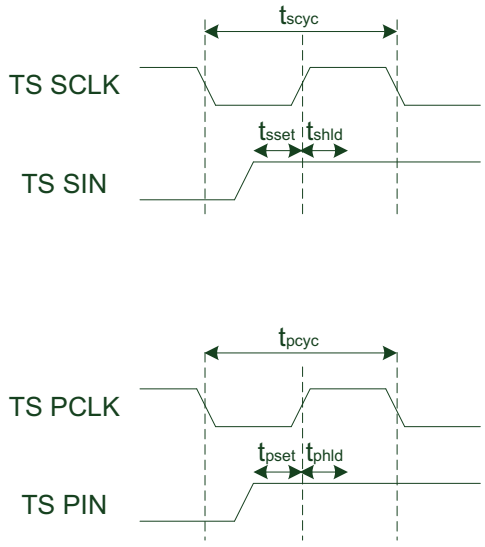


Figure 2.50. : TS timing of not inverted mode

2.5.15.2. TS CLK Inverted Mode

Table 2.62. : TS AC timing of TS clock inverted mode

Signal	Symbol	Description	Value			Unit
			Min	Typ	Max	
TS0CLK,TS1CLK (TS SCLK)	t_{scyc}	TS serial clock frequency	-	-	100	MHz
TS0CTL1, TS1CTL1, TS0CTL2, TS2CTL2 (TS SIN)	t_{sset}	Input signal setup time of serial mode	2	-	-	ns
	t_{shold}	Input signal hold time of serial mode	1	-	-	ns
TSCLK (TS PCLK)	t_{pcyc}	TS parallel clock frequency	-	-	AHB /6	MHz
TSDATA0,TSDATA1, TSDATA2, TSDATA3, TSDATA4, TSDATA5, TSDATA6, TSDATA7, TSCTL1, TSCTL2 (TS PIN)	t_{pset}	Input signal setup time of parallel mode	2	-	-	ns
	t_{phold}	Input signal hold time of parallel mode	1	-	-	ns
AHB : The AHB bus clock frequency is shown.						

At TsClk bit of TSD_INPUT_CFG register is 1, TS signal timing becomes the following.

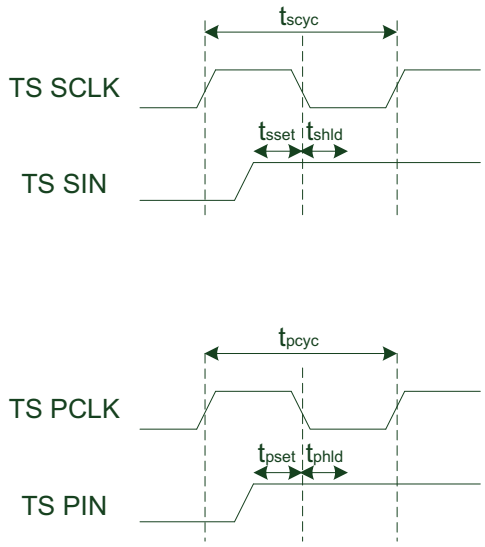


Figure 2.51. : TS timing of inverted mode

2.5.15.3. Host Interface Signal Timing

Table 2.63. : AC Timing of Host interface signals

Signal	Symbol	Description	Value			Unit
			Min	Typ	Max	
HOST_SCK	t_{cyc}	Clock Cycle time	20	-	-	ns
HOST_XCS	t_{cssr}	Chip Select setup time	1)	-	-	ns
	t_{cshr}	Chip Select hold time	1)	-	-	ns
HOST_DO	t_{do}	Data output delay time	3.0	-	8	ns
HOST_DI	t_{dsr}	Data input setup time	5	-	-	ns
	t_{dhr}	Data input hold time	0	-	-	ns
1): Please refer tp product specification (Host Interface chapter)						

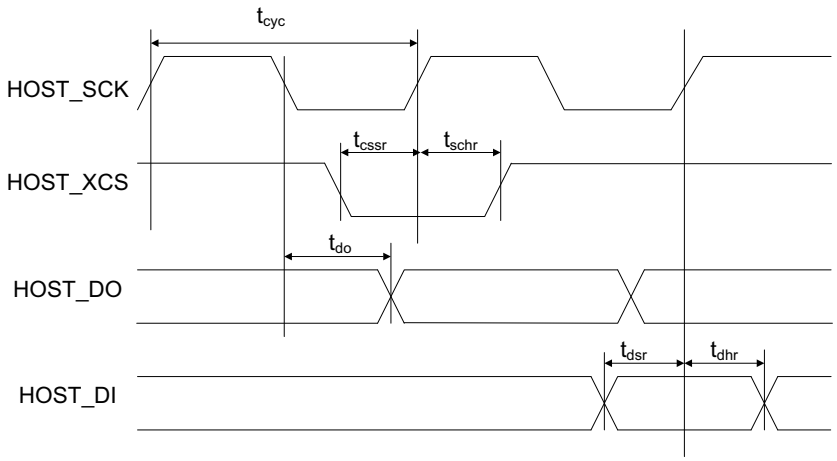


Figure 2.52. : Host I/F Timings

2.5.16. HS_SPI Signal Timing

Table 2.64. : HS_SPI Signal Timing

Signal Name	Symbol	Description	Value			Unit
			Min	Typ	Max	
HS_SCK	Tcyc	Clock Cycle time	-	-	66	MHz
HS_SSEL	Tcso	SSEL output delay time	-	-	2.5	ns
HS_SD[3:0]	Tdo	Data output delay time	-	-	4.5	ns
	Tdis	Data setup time	7.0	-	-	ns
	Tdih	Data hold time	0	-	-	ns

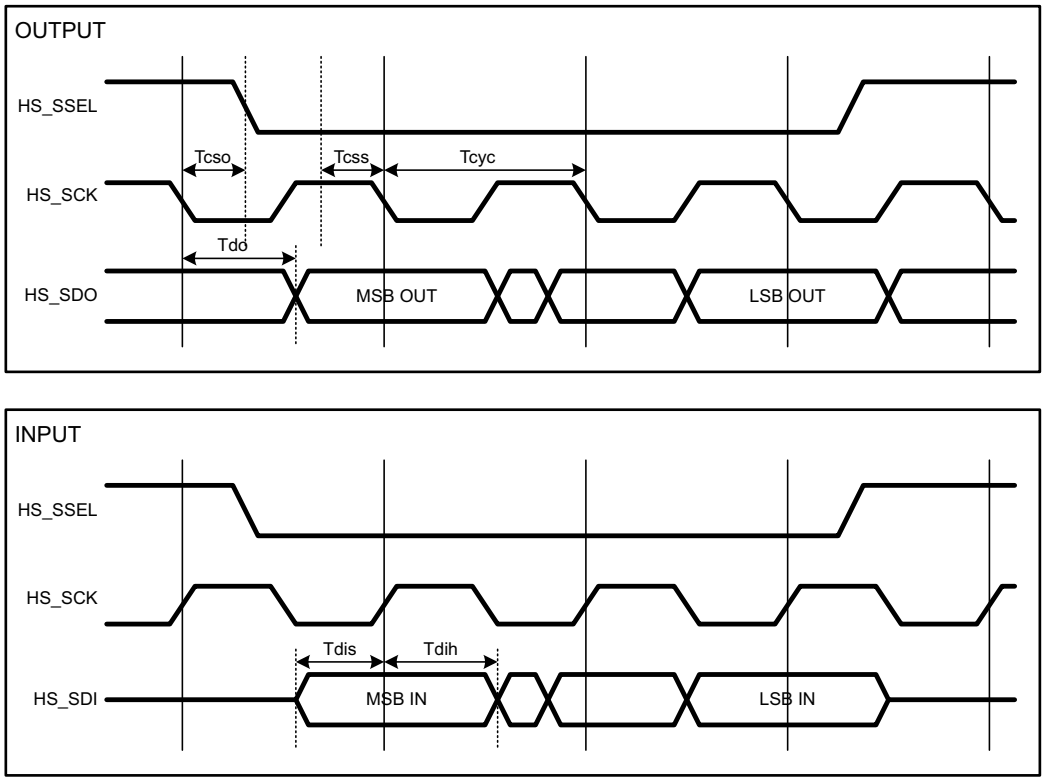


Figure 2.53. : HS_SPI signal timings

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