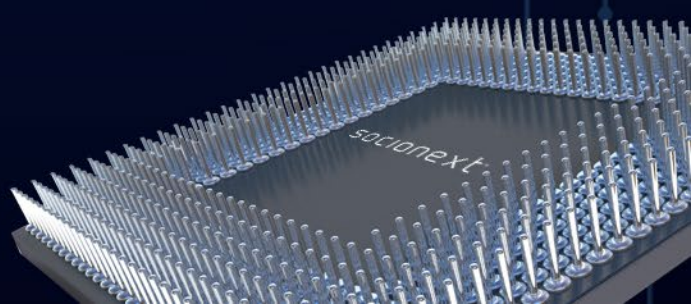
socionext™

WHITE PAPER

The Evolution of SerDes Architectures and Advantages of ADC-DSP for High-Speed Serial Communications



The advancement of high-speed serial communications has helped expand the Internet, and supercharged the growth in the storage, data center, and high-performance computing markets. Figure 1 shows the progress in serial communications since 1997, a 100x increase in serial data rates that has been driven by advances in SERDES (serializer-deserializer) technology.

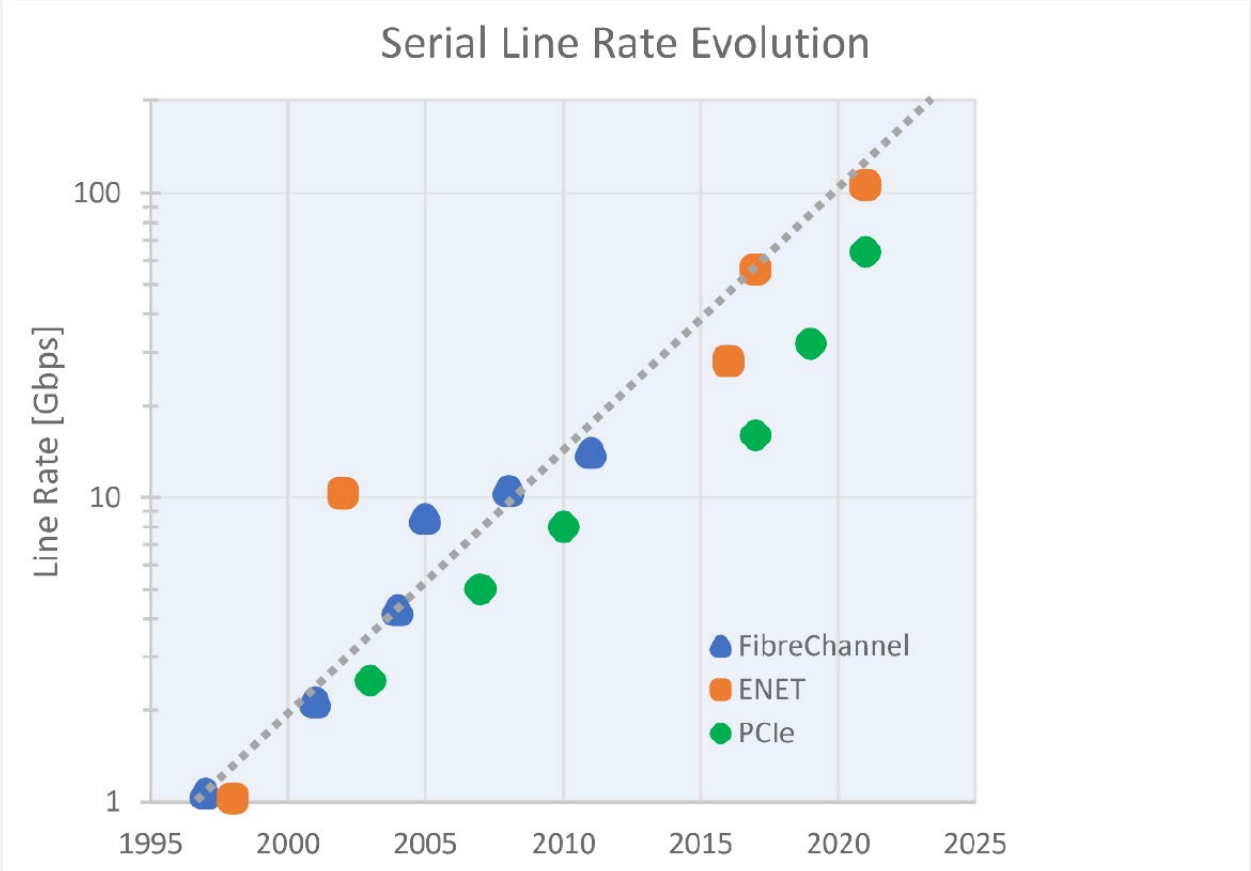


Figure 1: Evolution of Serial Line Rate.

The function of a SERDES, shown in Figure 2, is to multiplex parallel data into high-speed serial data for efficient transmission, and to receive and demultiplex high speed serial data to create lower speed parallel data for further processing.

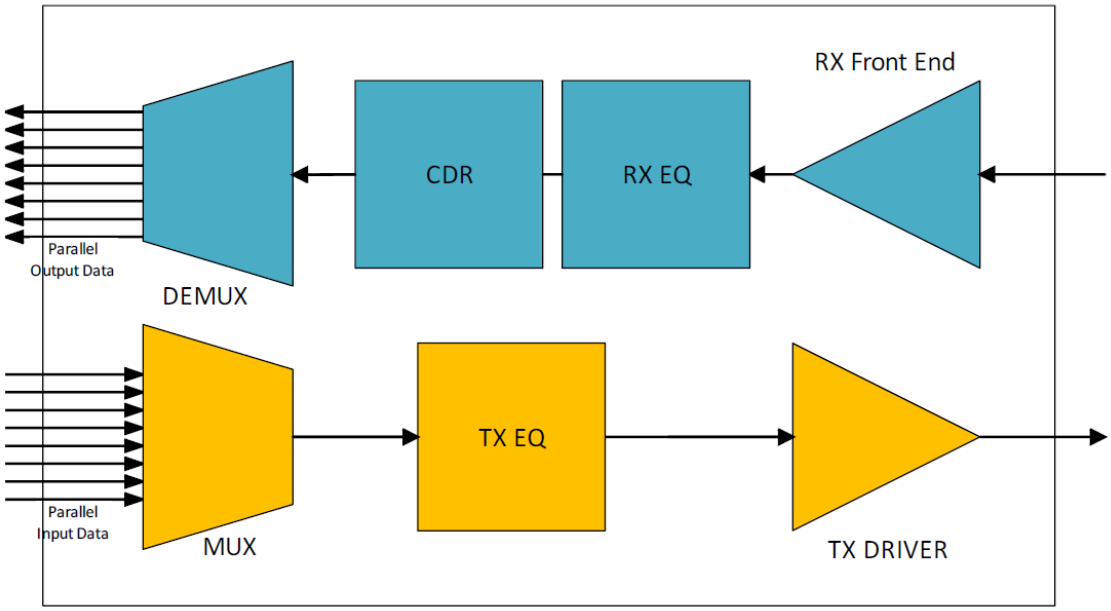


Figure 2. SERDES Block Diagram.

A key component of the SERDES RX (receiver) is the CDR (clock and data recovery), shown Figure 3a.

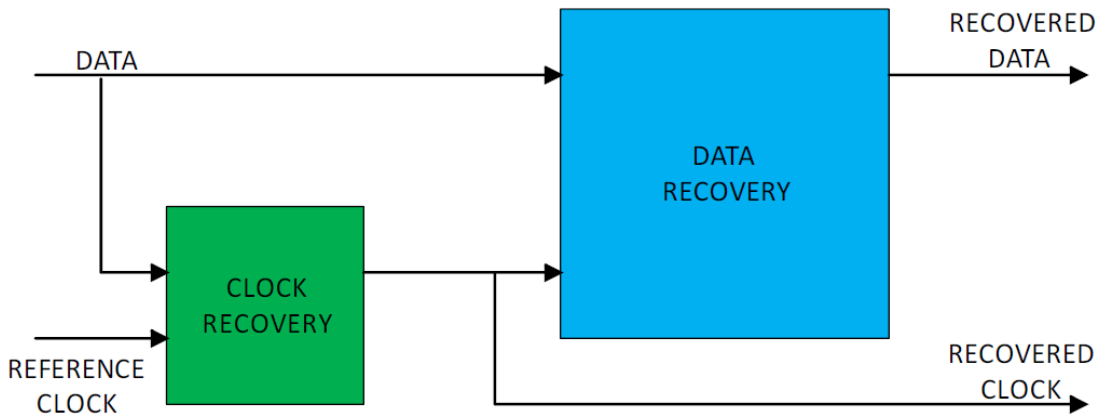


Figure 3a: Basic Clock Recovery Architecture

The purpose of the CDR is to extract, retime, and regenerate the received data stream. There are different CDR configurations: the linear CDR, shown in Figure 3b, and the non-linear CDR, shown in Figure 3c.

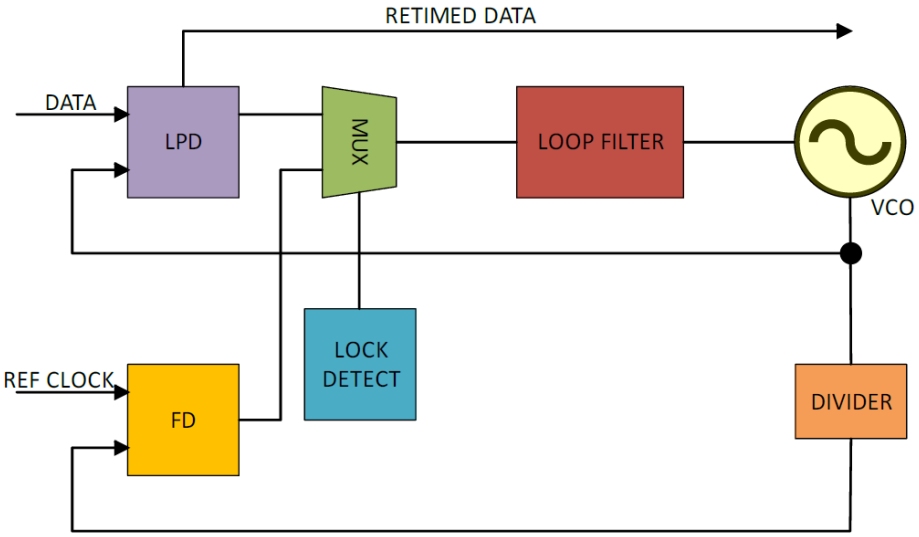


Figure 3b. Linear CDR Block Diagram. LPD (linear phase detector), FD (frequency detector). At startup, the CDR is locked to REF CLK. When initial lock is detected, the CDR is then locked to the input DATA.

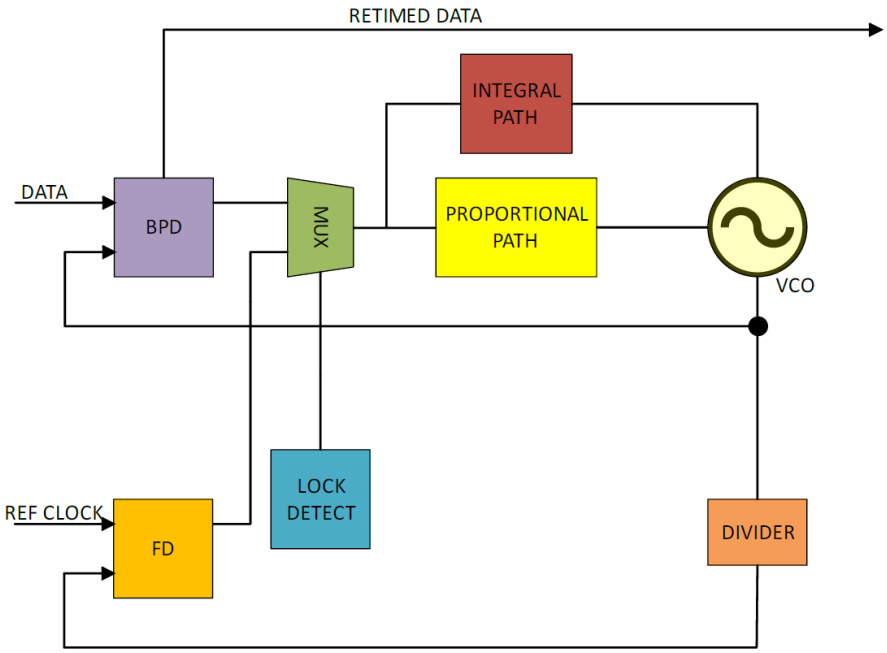


Figure 3c. Nonlinear CDR Block Diagram. BPD (binary phase detector), FD (frequency detector).

A linear CDR uses a linear phase detector to produce an error signal that is proportional to the difference between the incoming data and local clock. This error signal is integrated and filtered to align the VCO to the incoming data. The VCO clock is used to drive a decision circuit to regenerate the incoming data. A drawback of a linear CDR is that the alignment between data and clock produces very short duration phase detector pulses, which requires very fast analog circuitry. In addition, if the setup time of the phase detector flip-flops differ from the setup time of the retiming flip-flops, the data may not be sampled at the optimum point.

To avoid these drawbacks, a nonlinear CDR is used. A nonlinear CDR uses a bang-bang phase detector, which produces an error signal corresponding to the sign on the phase error (instead of the magnitude). A bang-bang phase detector uses three sample points, two located in adjacent data eyes, and one located at the transition. This optimally aligns the VCO clock with the incoming data.

High-speed data can be sent over a variety of transmission channels, and in this review, we will focus on transmission over a backplane, shown in Figure 4.

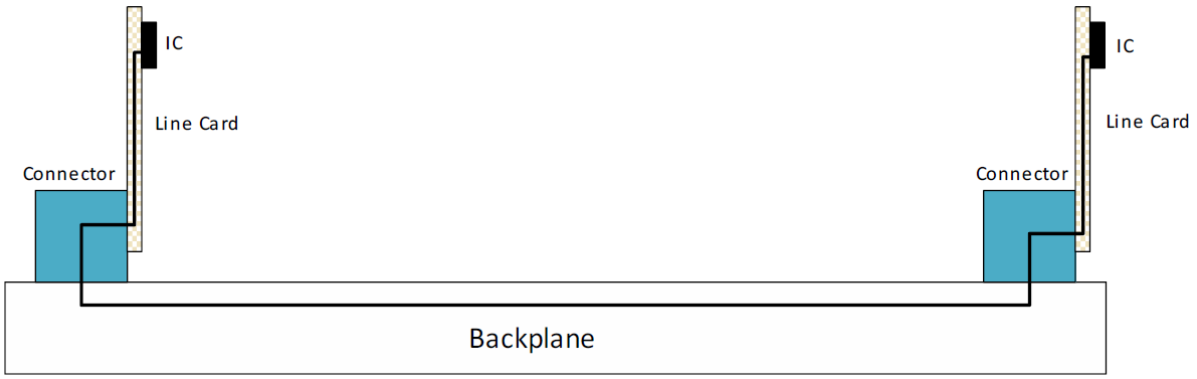


Figure 4: High speed serial data transmission through a backplane.

Signal transmission over a backplane is impaired by frequency dependent loss and impedance mismatch. As a result, it becomes more difficult for the CDR to accurately recover transmitted data. Backplane transmission channels can be characterized by their loss characteristics, which are related to the channel length. The insertion loss for typical short, medium, and long reach backplanes is shown in Figure 5.

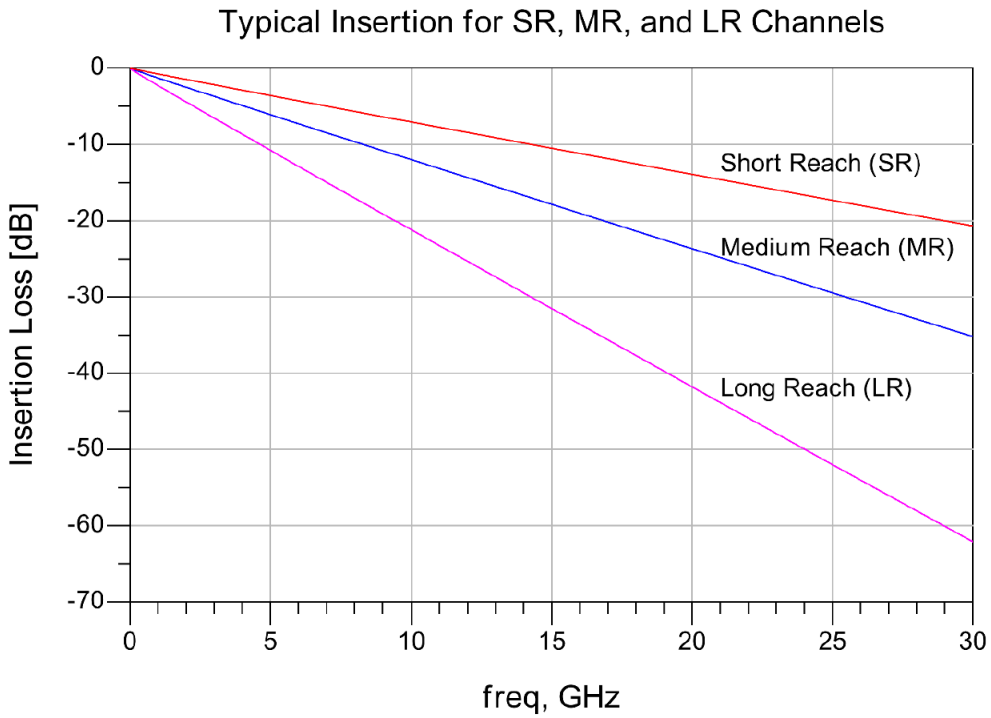


Figure 5: Insertion loss characteristics for short reach (SR), medium reach (MR), and long reach (LR) channels.

The channels of Figure 5 are created mathematically using a physical transmission line model that has frequency dependent loss but does not have impedance mismatch. As serial data rates increase, and as the channel length increases, data transmission becomes subsequently more difficult. This can be visually characterized by simulating, with the Keysight ADS channel simulation toolbox, the data eye diagram after passing through a transmission channel. These simulation results are shown in Figure 6.

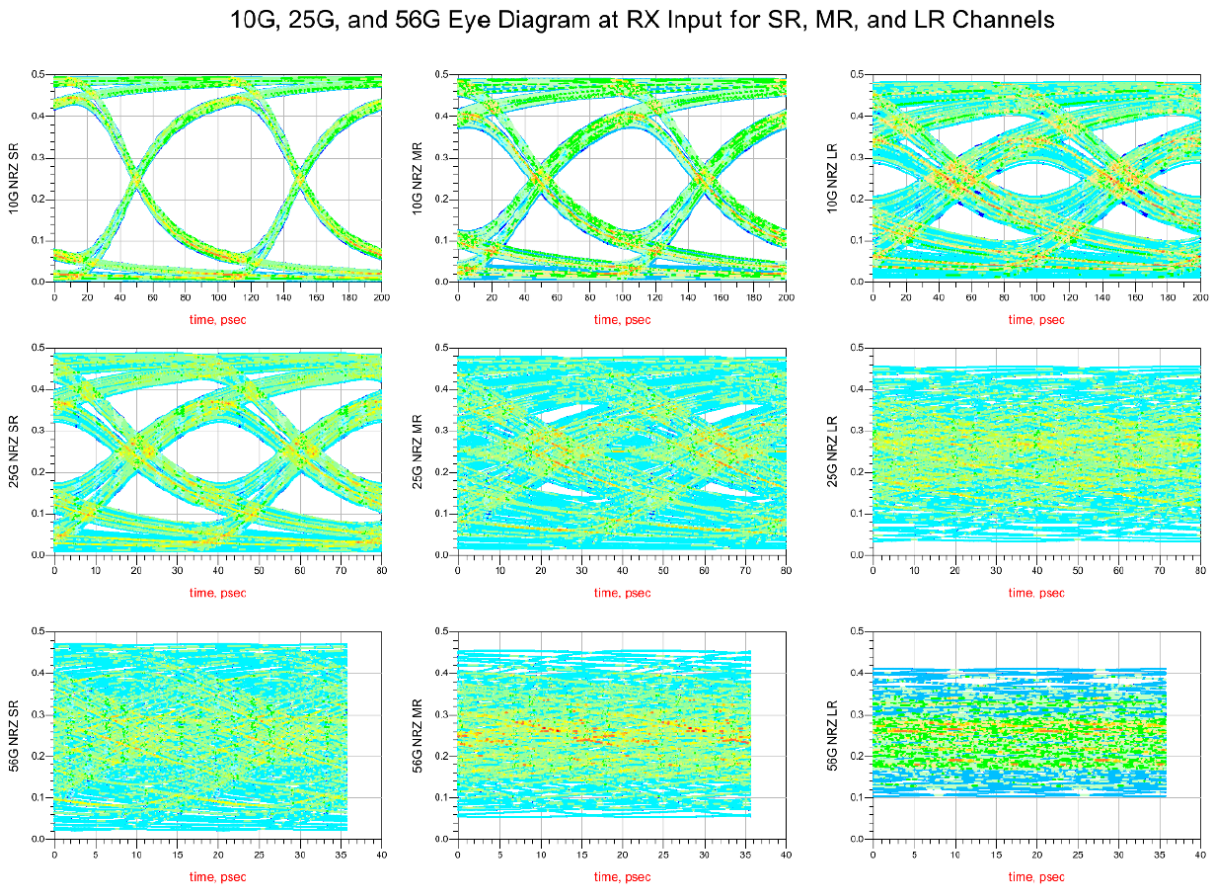


Figure 6. Eye Diagrams at 10G, 25G, and 56G data rates for SR, MR, and LR channels.

The transmitted data is in NRZ format (non-return to zero) which has two levels that represent either a logical 1 or logical 0. For 10G transmission through a short channel, the data eye is relatively undistorted. However, as the data rate increases, and as the channel loss increases, the data is significantly distorted. In many cases, the data eye is completely closed.

Mitigating the detrimental effects of channel transmission requires some form of equalization. Equalization can be performed at either the TX or RX with a FFE (feed forward equalizer), and at the RX, with CTLE (continuous time linear equalization) and DFE (decision feedback equalizer).

FFE is implemented by creating a series of delayed and scaled versions of the input signal that are summed together to create the equalized signal. The delay value is 1 UI (unit interval). This is the same structure as a transversal finite impulse response (FIR) filter. A typical implementation of FFE is shown in Figure 7. When implemented at the TX, FFE is also called pre-emphasis or TX FIR.

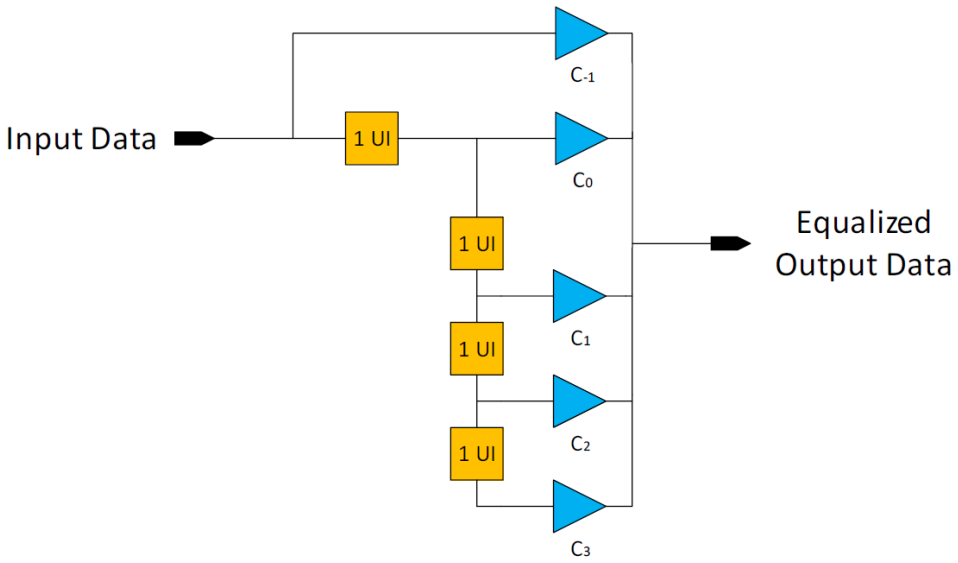


Figure 7. FFE Implementation.

A backplane attenuate signals, and the loss increases with increasing frequency. CTLE compensates for channel loss by boosting higher frequencies at the receiver. A CTLE implementation using a source degenerated differential amplifier is shown in Figure 8a.

This circuit has two poles and one zero, and the frequency response is tuned by setting the DC gain and the pole/zero location, as shown in Figures 8b and 8c. The CTLE settings are adjusted for optimal performance based on the loss characteristics of the transmission channel and the data rate.

CTLE and FFE are linear forms of equalization, and work well in compensating for channel loss. However, a backplane can also impair signal transmission with reflections created by impedance mismatch. To compensate for this impairment, DFE is required. DFE compensates the received signal by feeding back a weighted version of the detected signal, which is either a 1 or 0. The feedback shifts the signal before the detector depending on the detected bit. With DFE, the feedback signal is binary and discrete. A typical DFE implementation is shown in Figure 9. FFE and CTLE are typically used to condition the RX signal before DFE is applied.

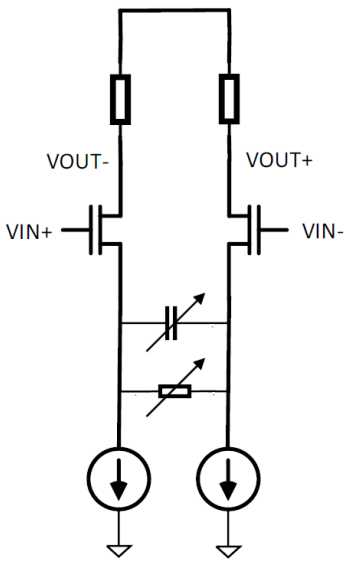


Figure 8a. CTLE implementation with a source degenerated differential amplifier. The pole and zero locations are adjusted by tuning the R and C in the amplifier.

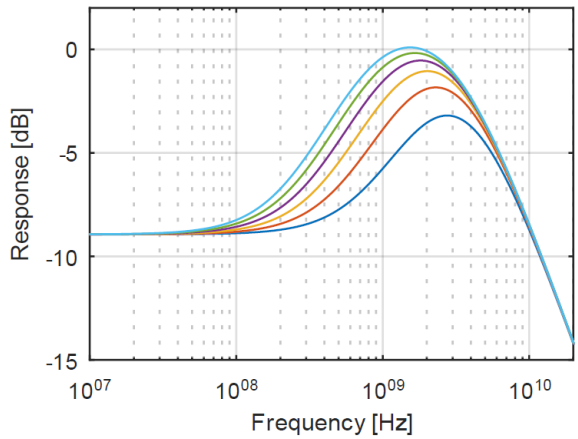


Figure 8b. RX CTLE Equalization. CTLE compensates for frequency dependent channel loss by creating a frequency response that increases gain at higher frequencies. This frequency response is calculated from the circuit of Figure 8a. The value of the tunable capacitor is swept to adjust the location of the peak.

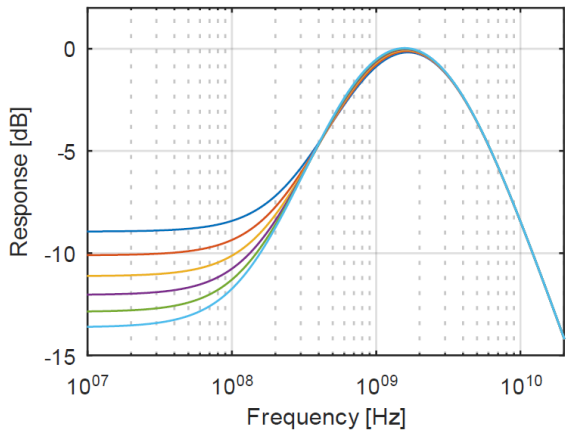


Figure 8c. RX CTLE Equalization. CTLE compensates for frequency dependent channel loss by creating a frequency response that increases gain at higher frequencies. This frequency response is calculated from the circuit of Figure 8a. The value of the tunable resistor is swept to adjust the low frequency attenuation.

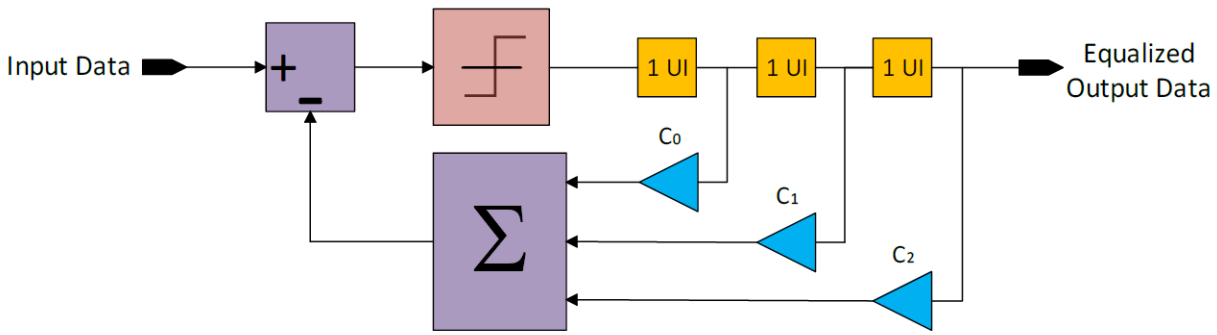


Figure 9. A typical DFE implementation.

Data transmission and the benefits of equalization can be further explored by looking at a real backplane channel. The measured characteristics of 29.8” backplane channel are shown in Figure 10.

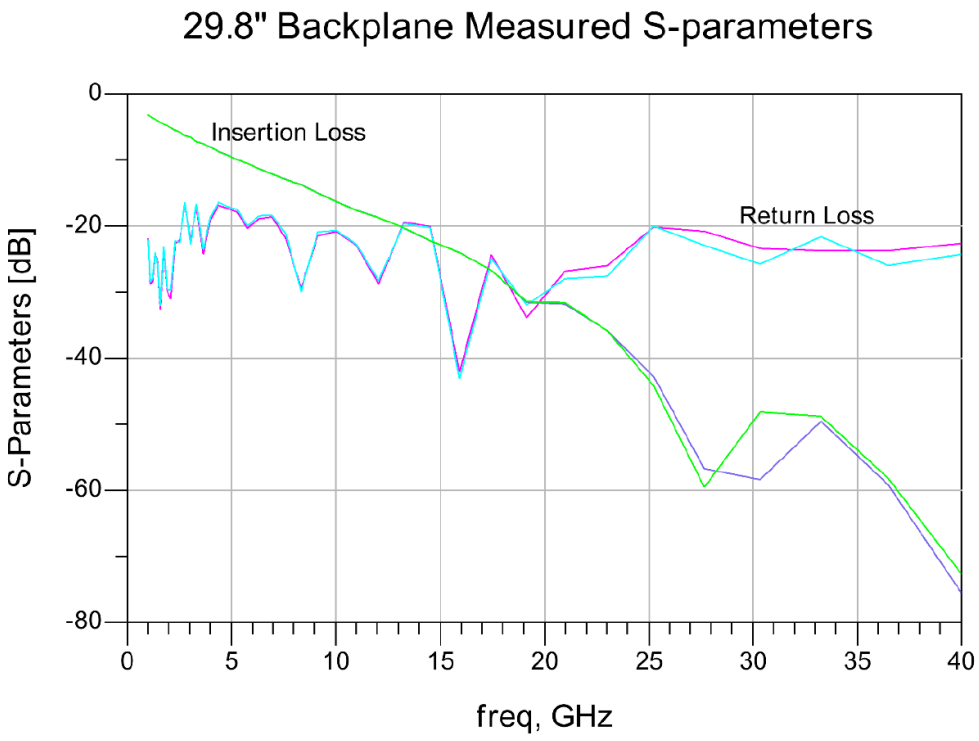


Figure 10. Measured characteristics of a 29.8” backplane.

This data is publicly available at https://www.ieee802.org/3/100GCU/public/channel.html. This channel has both frequency dependent insertion loss and impedance mismatch. Data transmission through this channel is simulated using the testbench shown in Figure 11, and the results are shown in Figure 12.

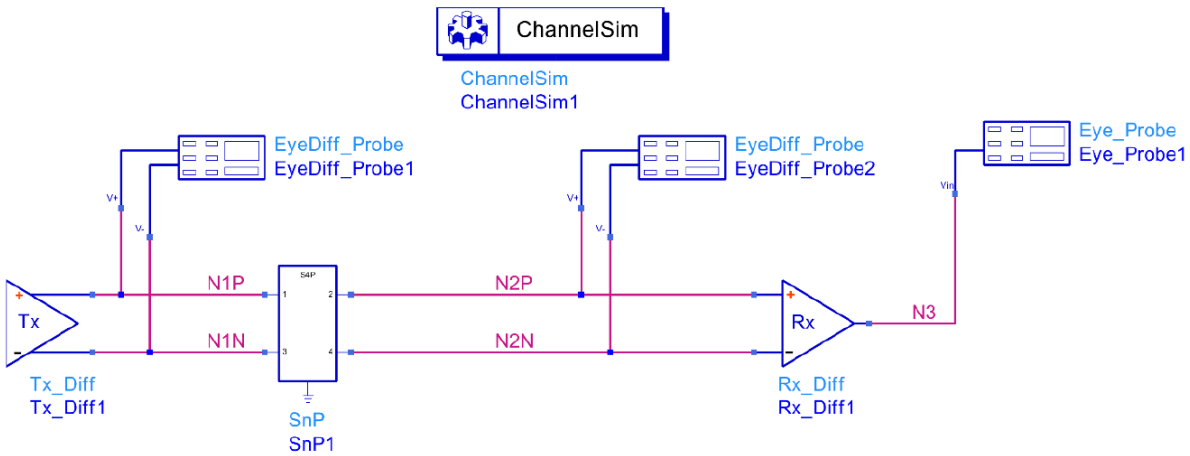


Figure 11. Keysight ADS simulation schematic

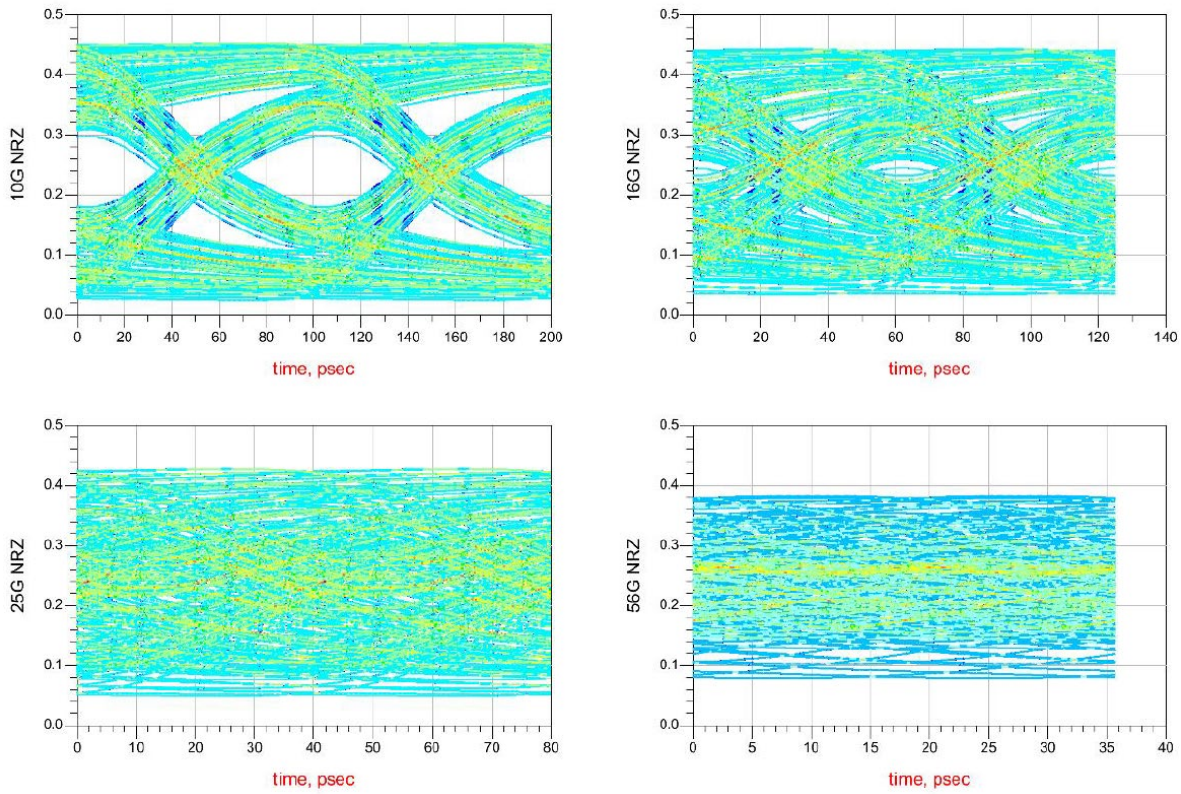


Figure 12. Unequalized NRZ transmission through a 29.8" backplane channel is shown above for 10G, 16G, 25G, and 56G data rates. After 10G, the data eye diagram is closed, and equalization is required to recover the data at the RX.

At 10G, there is a distorted but partially open data eye. Beyond 10G, the data eye is completely closed. This situation can be improved with equalization, and the effects of FFE, FFE+CTLE, and FFE+CTLE+DFE for 10G, 16G, 25G, 32G, and 56G NRZ data transmission are shown in Figures 13a through 13e. For 10G and 16G transmission, FFE alone is sufficient to create an open data eye. For 25G and 32G transmission, DFE must be used to increase the data eye opening. At 56G, even FFE+CTLE+DFE is insufficient to create an open data eye.

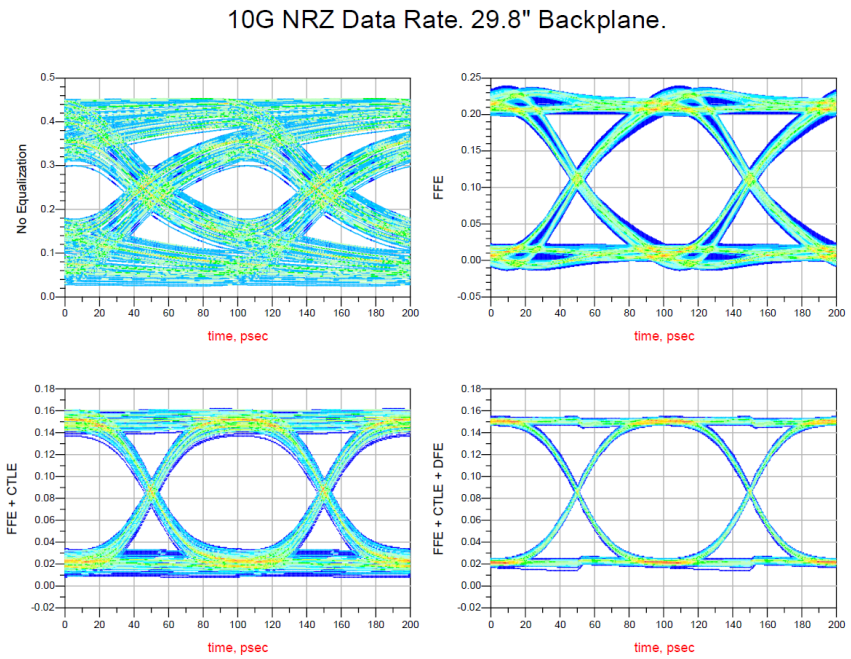


Figure 13a. The effect of equalization on a 10G NRZ data transmission through a 29.8" backplane channel. FFE is sufficient to create an open eye diagram. As additional equalization is applied, the quality of the data eye continues to increase.

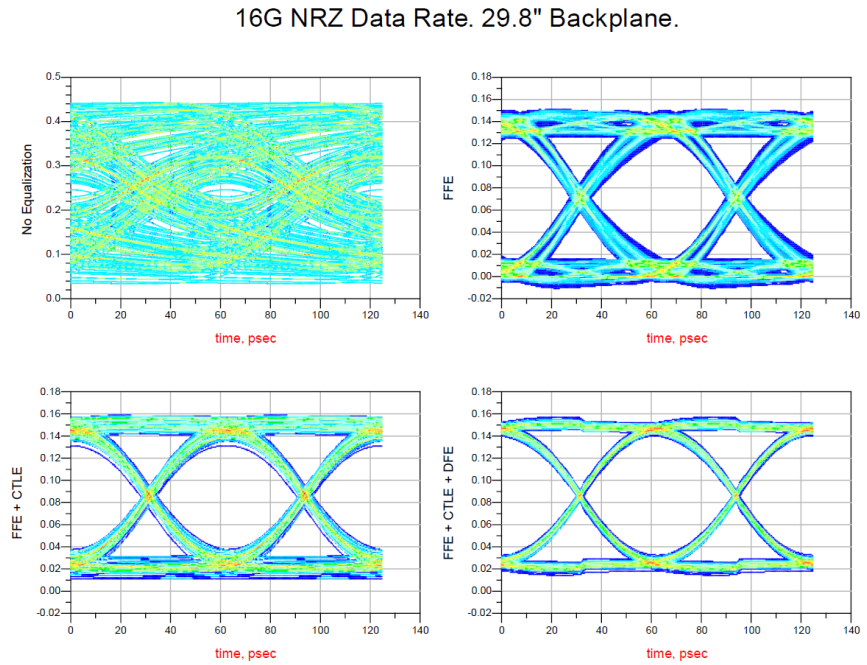


Figure13b. The effect of equalization on a 16G NRZ data transmission through a 29.8" backplane channel.

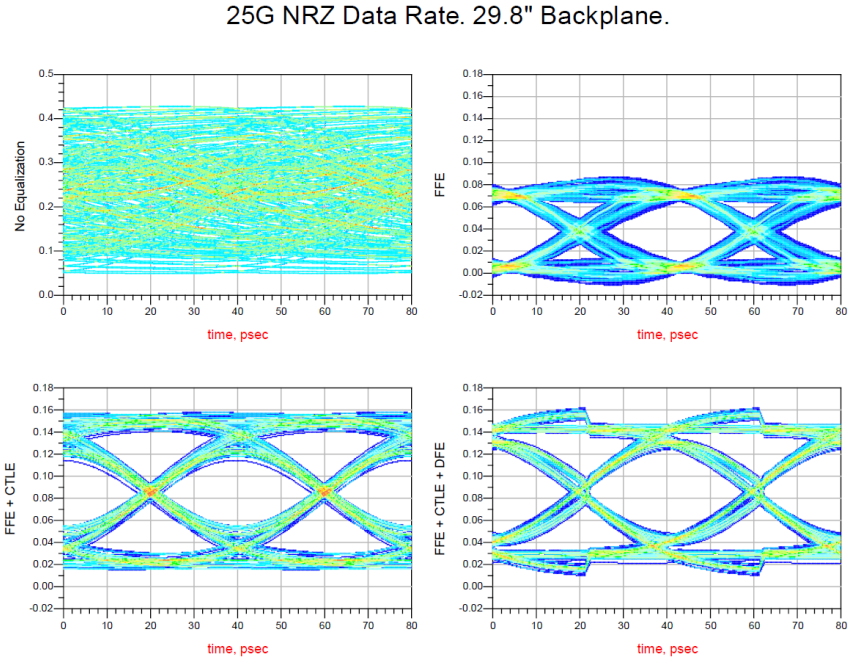


Figure 13c. The effect of equalization on a 25G NRZ data transmission through a 29.8" backplane channel. A combination of FFE and CTLE creates an open data eye. As additional equalization is applied, the quality of the data eye continues to increase.

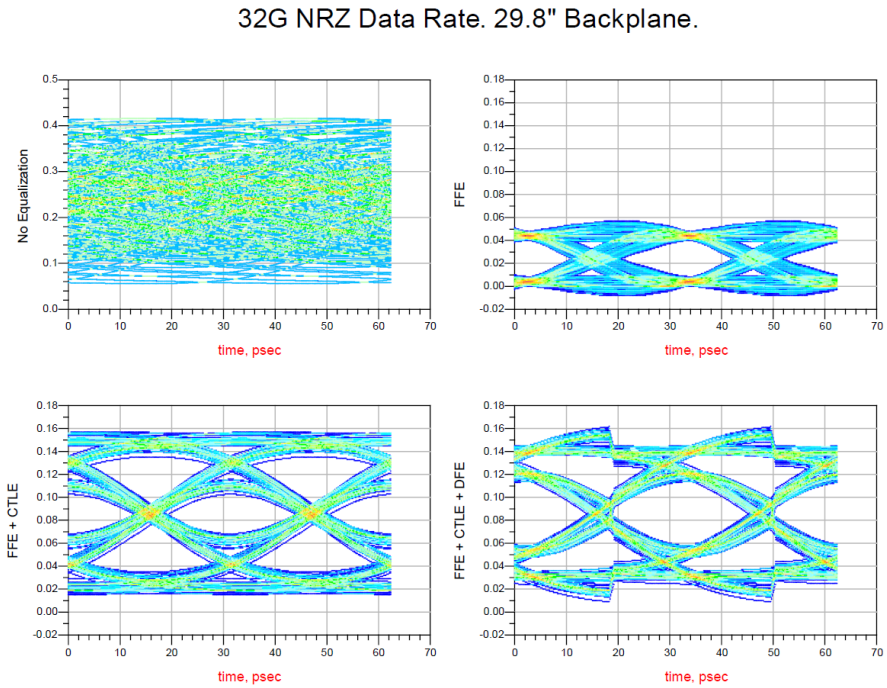


Figure 13d. The effect of equalization on a 32G NRZ data transmission through ugh a 29.8" backplane channel. DFE is required to increase the data eye opening for accurate data recovery.

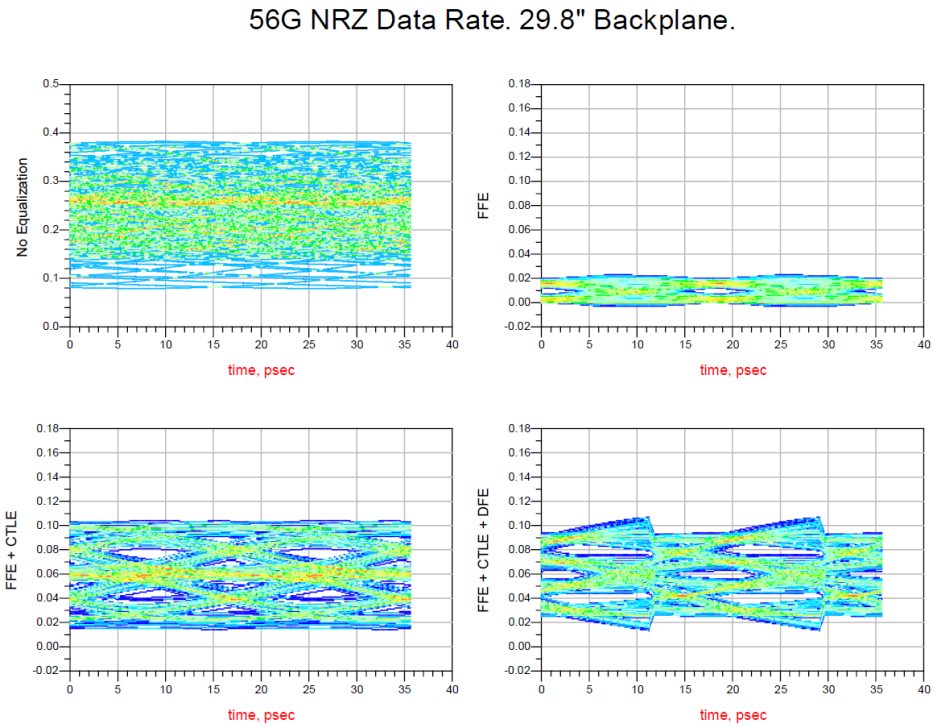


Figure 13e. The effect of equalization on a 56G NRZ data transmission through a 29.8" backplane channel. Here, the application of FFE, CTLE, and DFE is insufficient to create an open data eye.

To continue increasing serial data rates, PAM4 signaling, shown in Figure 14, has been introduced.

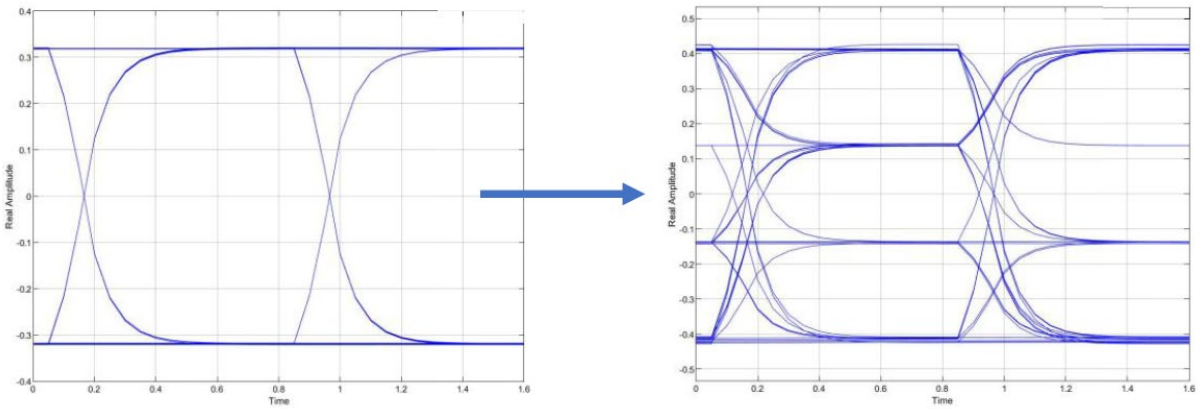


Figure 14. PAM4 Signaling. Instead of using 2-levels to represent a logical '0' and '1' (NRZ), PAM4 uses 4 levels to represent '00', '01', '10' and '11'.

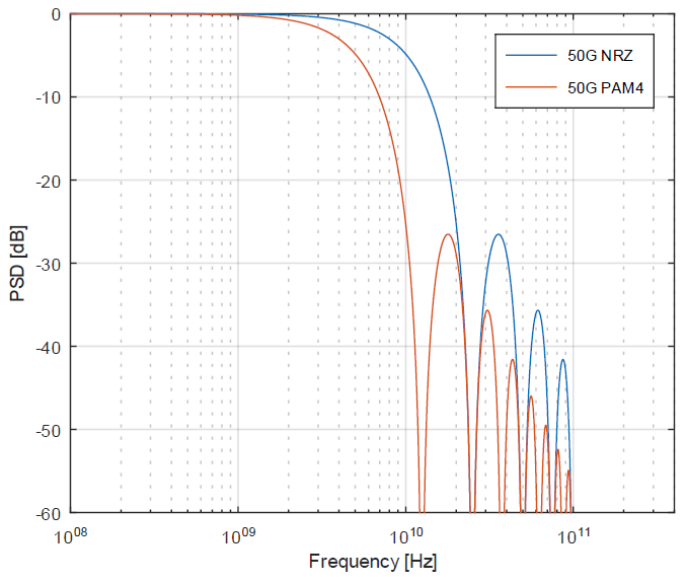


Figure 15. NRZ and PAM4 Power Spectral Density (PSD) comparison. Because PAM4 has two symbols at each transition, the spectrum of a PAM4 signal is comparable to the spectrum of an NRZ signal of twice the data rate.

When compared to NRZ signaling, the levels of PAM4 are 1/3 that of NRZ, and thus PAM4 has 9.5 dB lower SNR. However, the signal spectrum of PAM4 is comparable to an NRZ signal of half the data rate, as shown in Figure 15.

In cases where the channel loss at the Nyquist frequency of an NRZ signal is greater than 9.5 dB of the channel loss at Nyquist for a PAM4 signal, then PAM4 signaling has an advantage. For example, with the medium reach channel in Figure 5, a 56 Gbps NRZ signal has a Nyquist frequency of 28 GHz, and a channel loss of -34dB. A 56 Gbs PAM4 signal has a Nyquist frequency of 14 GHz, with a channel loss of -17dB. In this case, PAM4 signaling is advantageous.

A conventional SERDES RX architecture that uses the CDR structures in Figure 3b or 3c cannot be used to recover PAM4 data. Multi-level transmission requires a new SERDES RX architecture, based on using an ADC (analog to digital converter), shown in Figure 16.

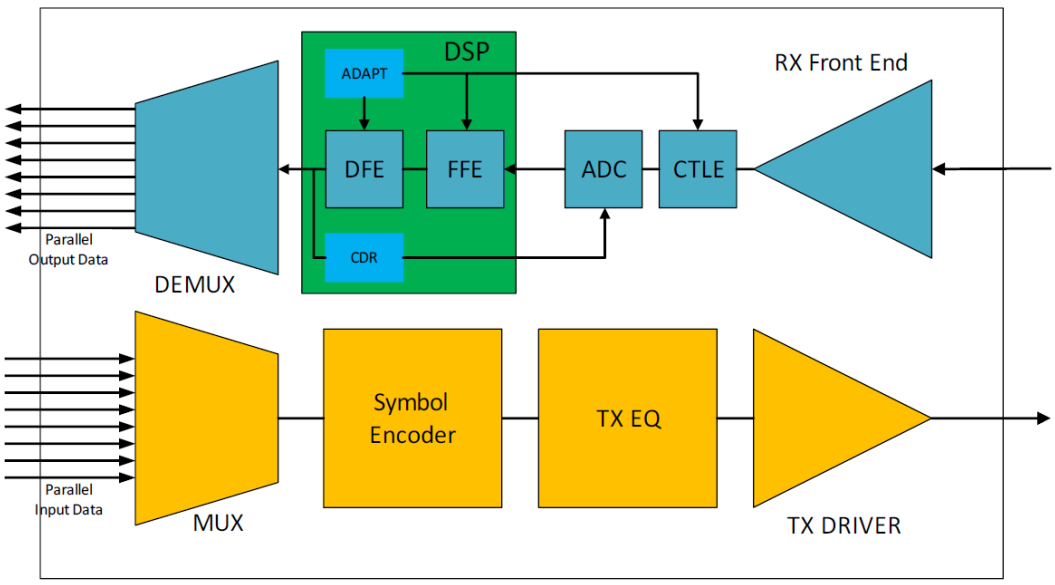


Figure 16. ADC SERDES Block Diagram. In the TX, a symbol encoder is used to generate PAM4 data. In the RX, an analog to digital converter (ADC) is used to sample the input data, which is then equalized with a combination of FFE and DFE within the DSP block. In the DSP block, adaption and clock and data recovery is also performed.

As described above, an ADC-DSP SERDES architecture has several advantages over a conventional SERDES architecture:

- Ability to handle multi-level signaling, such as PAM4, PAM8, etc…
- Ability to implement complex equalization algorithms using DSP
- Improved robustness to PVT variation
- Scales well as CMOS dimensions shrink
- Can still be combined with linear equalization, CTLE and FFE

These benefits when applied deliver reliable data dependably at ever increasing rates. The progress since 1997 continues.

socionext™

The Evolution of SerDes Architectures and Advantage on ADC-DSP for High-Speed Serial Communications

 | sna_inquiry@us.socionext.com