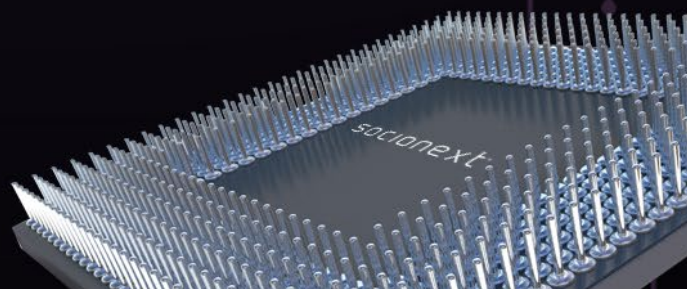
socionext™

WHITE PAPER

How an ADC-DSP Architecture Can Enable Increased Serial Data Rates



Note to readers:

There are two previous articles to this series. First article reviewed the SerDes architecture for NRZ transmission and the limitations of NRZ (non-return to zero) transmission as data rates increase, and the need for PAM4 (Pulse Amplitude Modulation) transmission to continue the increase in serial line rate. The second article of the series compares NRZ and PAM4 data transmission by simulating data transmission through a 29.8" backplane channel.

For this third part, we will explore the use of ADC-DSP SerDes architecture to effectively handle continued increase in serial line rates.

The NRZ SerDes transmitter architecture can be readily adopted for PAM4 transmission. However, the receiver architecture, in particular the CDR (clock data recovery), cannot be effectively adapted for PAM4 transmission. This is because PAM4 signals have multiple transition amplitudes, as shown below in Figure 1.

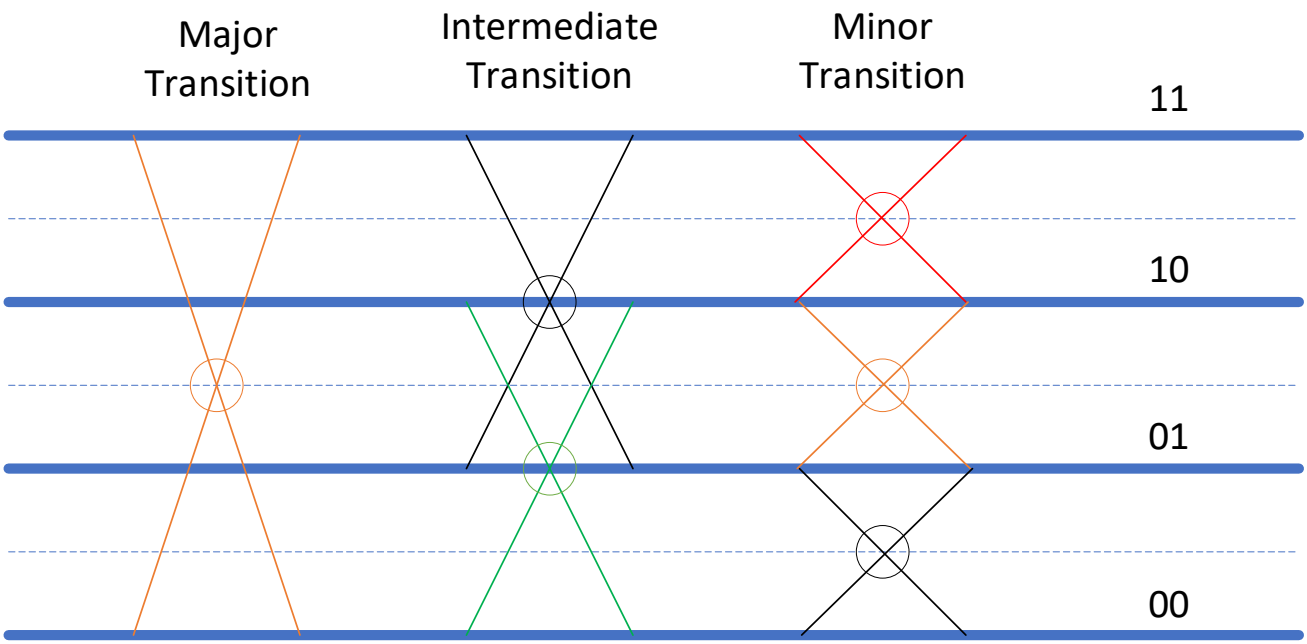


Figure 1. Transitions for PAM4 signaling. The major transition is the change between 00 <-> 11. The intermediate transitions are the changes between 00 <-> 10, and 01 <-> 11. The minor transitions are the changes between 00 <-> 01, 01 <-> 10, and 10 <-> 11.

While NRZ signals have a single major transition, a PAM4 signal has six transitions. These transitions consist of one major transition, two intermediate transitions, and three minor transitions. A conventional NRZ CDR architecture is designed to utilize a single transition type for clock recovery. If an NRZ CDR is used for PAM4 signaling, the multiple transition types and transition amplitudes create difficulties in obtaining CDR lock. For a CDR to effectively lock onto a PAM4 signal, all six transitions need to be used to extract the clock from the incoming data. This requires a new architecture, the ADC-DSP based receiver, shown in Figure 2.

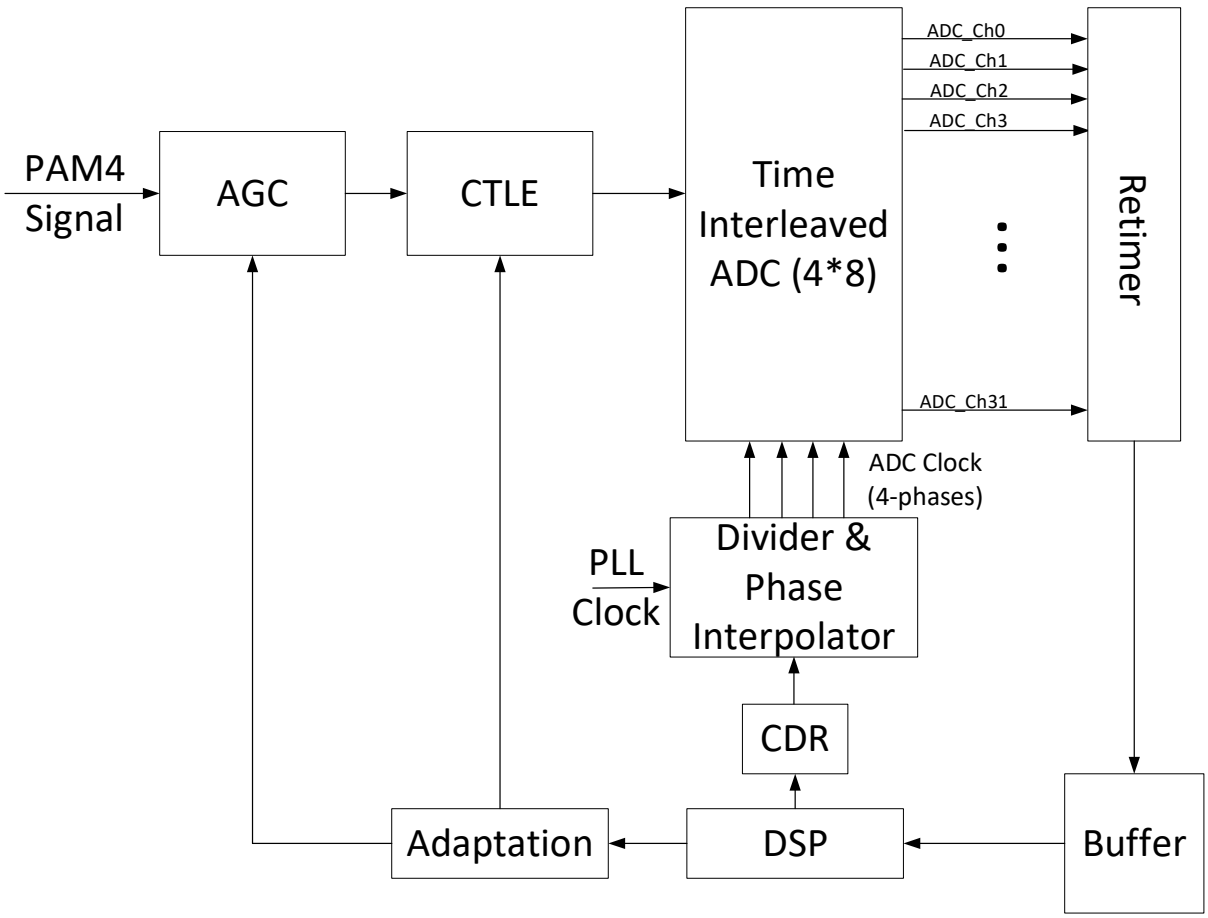


Figure 2. **ADC-DSP Receiver Block Diagram. The specific receiver shown here is implemented with a 4*8 ADC configuration, i.e., 4 parallel and interleaved ADC blocks, with 8 sub-ADC blocks in each ADC. The ADC is driven by a 4-phase clock that is generated from the PLL clock. The ADC configuration can be adjusted based on the desired ADC clock speed.**

The ADC-DSP receiver of Figure 2 has an analog front end comprised of an AGC (automatic gain control) amplifier and CTLE equalization, followed by a time interleaved ADC (analog-to-digital converter) stage. The ADC is a SAR (successive approximation register) type. A SAR ADC has the advantage of minimizing space requirement but is limited in its operating speed. In order to sample a high-speed input signal, parallel and interleaved ADC stages are implemented. The ADC stages are clocked with a phase shifted version of the PLL (phase lock loop) clock. This is shown in Figure 3, in which the ADC has four parallel stages, clocked by 0, 90-, 180-, 270-degree phases of the PLL clock.

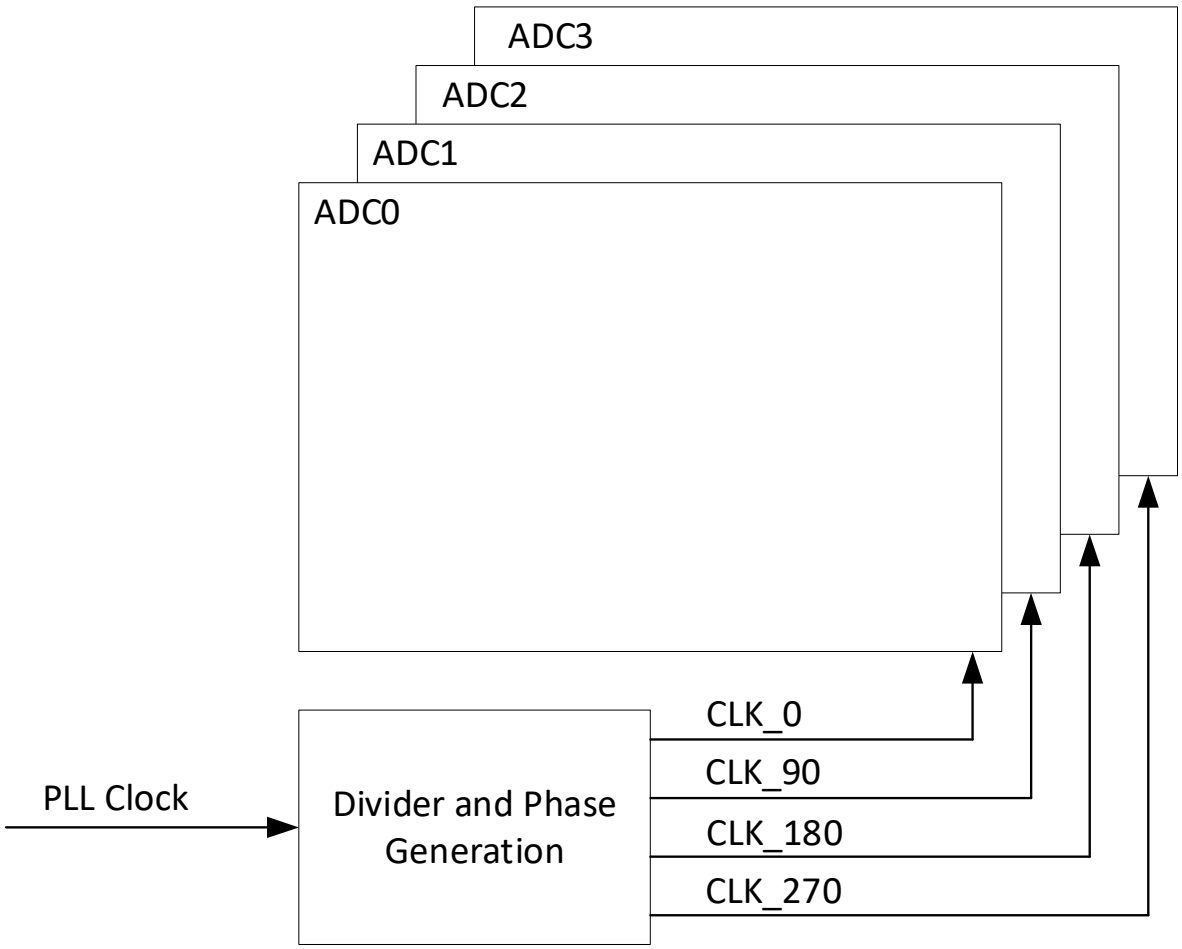


Figure 3. Parallel ADC Implementation. In this case, four parallel ADC blocks are implemented, and clocked with four equally spaced (90 degree) phases of the PLL clock.

To further ease speed requirements and avoid the complication of generating a large number of phases from a single clock, each ADC stage can be implemented as a set of parallel sub-ADCs, as shown in Figure 4. To operate the sub-ADC blocks, further clock phase generation occurs locally within in each ADC. In Figure 4, the ADC block contains eight sub-ADC stages, clocked by the 0, 45-, 90-, 135-, 180-, 225-, 270-, and 315-degree clock phases. The receiver shown in Figure 2 is in the 4*8 ADC configuration, with 4-parallel ADC stages, and each ADC stage implemented with 8 sub-ADC stages. Four phases, with 90 degrees spacing, are generated from the main PLL clock. In each ADC block, 8 additional phases with 45 degrees spacing are generated. This approach to clock phase generation is more accurate than having to generate 32 clock phases, with 11.25 degree spacing, from a single clock.

The interleaved and parallel implementation greatly reduces the speed requirements of the ADC. For example, to receive a 56 Gb/s PAM4 signal, each ADC unit operates at 875 MHz. Higher serial data rates can be received by either operating the ADC with a faster clock, or increasing the number of parallel ADC stages, or by increasing the number of sub-ADC blocks. For example, a 112 Gb/s PAM4 receiver can also use a 4*8 ADC configuration with each ADC unit now clocked at 1.75 GHz. An 875 MHz ADC clock can be maintained with an 8*8 or a 4*16 ADC configuration. The 8*8 configuration is advantageous since the minimum clock phase spacing will remain at 45

degrees, while the 4*16 configuration requires a minimum clock phase spacing of 22.5 degrees. The ability to configure the ADC into parallel ADC blocks and sub-ADC units allows for higher serial data rates to be received without excessively increasing the speed of the ADC clock.

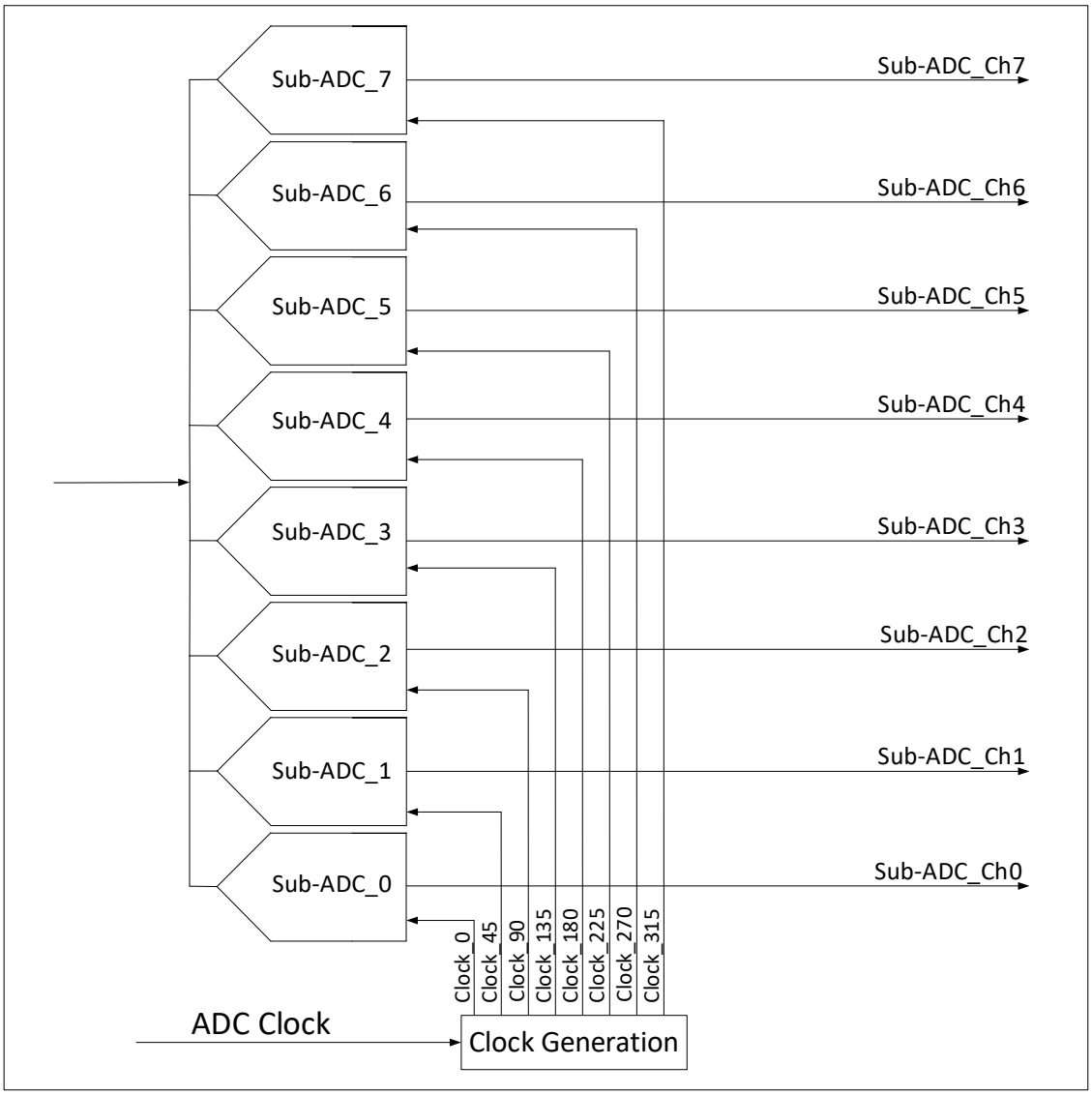


Figure 4. Sub-ADC Implementation within each ADC unit. In this case, 8 sub-ADC units are implemented and clocked with 8 equally spaced (45 degree) phases of the ADC clock.

After being sampled by the ADC, the parallel data is retimed, stored in a buffer and then processed in the DSP (digital signal processing) circuitry to recreate the PAM4 signal. The DSP is implemented in a parallel manner, which matches the parallel ADC data. Additional feed forward equalization is applied in the DSP. This data is sent to the CDR loop, which is also implemented digitally. The clock recovery algorithm detects minor, intermediate, and major data transitions. Further equalization in the form of DFE is applied in the CDR algorithm. For a DSP based CDR, the optimal equalization configuration is often a 1-tap DFE with a large number (24 to 40 or more) of FFE taps. The output signal from the CDR is used to drive a phase interpolator, which aligns the PLL clock with the incoming data. The adaptation of the receiver equalizer settings is performed digitally, and optimal receive settings can be found during a training sequence when the communications link is established. DSP allows for

sophisticated signal processing algorithms to be implemented and applied to the incoming PAM4 data. This allows for mitigation of complex channel impairments, such as multiple reflections due to impedance mismatch, high channel loss, and crosstalk. With DSP, low BER (bit error rate) signal transmission can be achieved even in difficult environments.

In the ADC-DSP SerDes architecture, only the CTLE, AGC, and TX driver stages need to operate at the serial line rate. These are low transistor count analog circuits that can readily be scaled to operate at high frequencies. The interleaved and parallel configuration allows the ADC, DSP and CDR circuitry to operate at much lower frequencies. The use of DSP allows complex equalization and clock recovery algorithms to be implemented. In addition, the ADC-DSP SerDes has greatly improved robustness to PVT variation, and scales well as CMOS dimensions shrink. By modifying the DSP, this architecture can handle higher level modulation formats such as PAM6 and PAM8. The ADC-DSP SERDES architecture provides a practical path forward for continued increase in serial line rates.

socionext™

How an ADC-DSP Architecture Can Enable Increased Serial Data Rates