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Expectations & Initiatives for Automotive Chiplets

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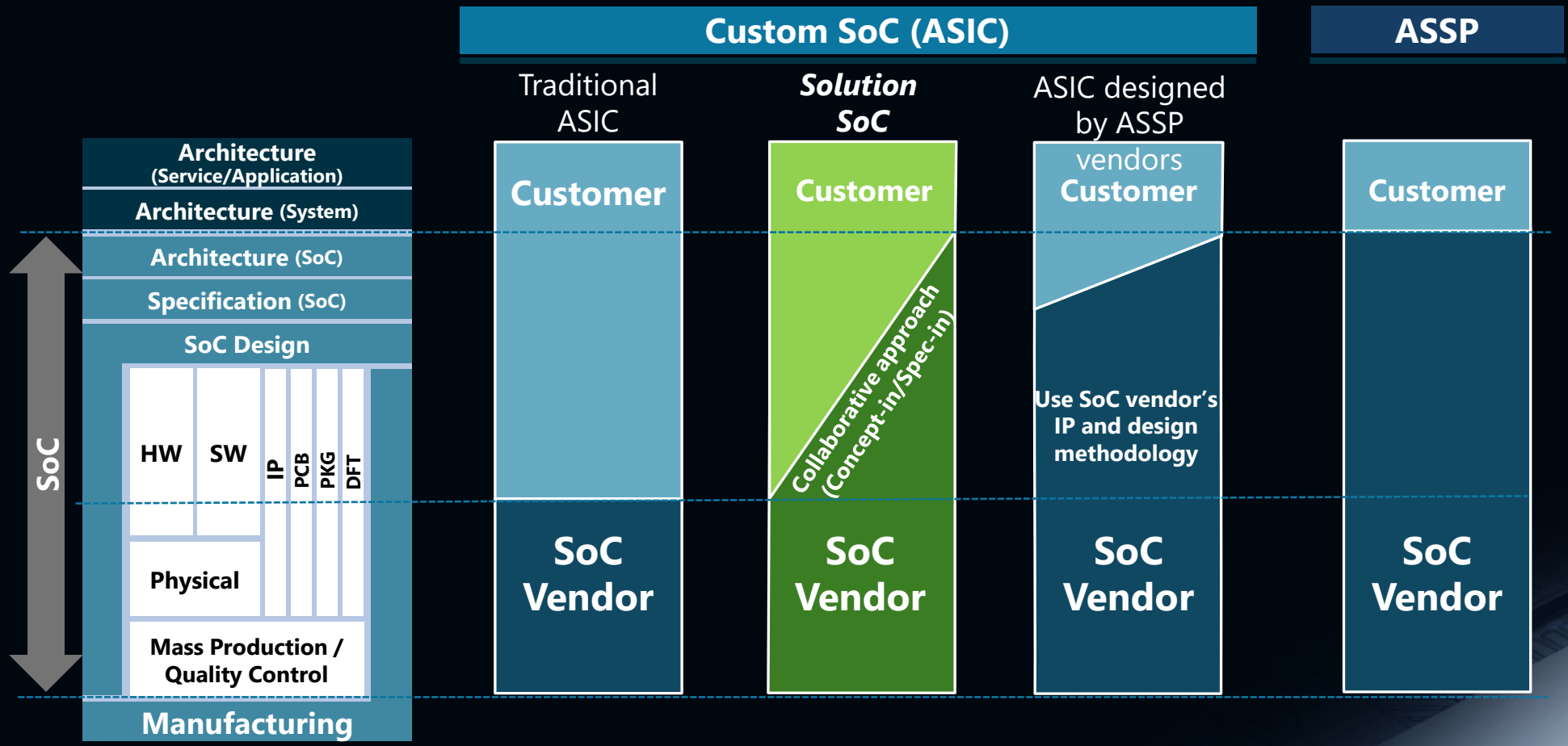
Agenda

- The Socionext “Solution SoC” Approach to Designing Automotive Chiplets
- Automotive SoC Components and Chiplet Requirements
- Expectation and Challenges for 2.5D/3D Chiplets
  - Design
  - Fabrication
- Call to Action

What is Socionext's "Solution SoC"?

The primary difference between traditional ASIC and Solution SoC is how we interface with customers
The major difference between Solution SoC and ASIC designed by ASSP vendors is the ***breadth of optional customization***



Expanding “Solution SoC” to Automotive Chiplets

- Subsystem configurations and bus architectures are becoming similar across major applications
- Building a common design platform improves development efficiency and profitability

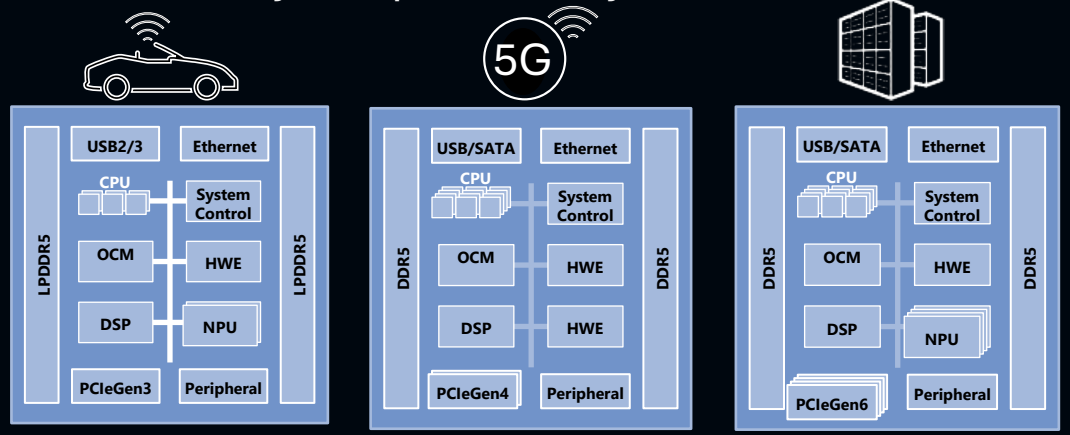
Socionext’s standard approach

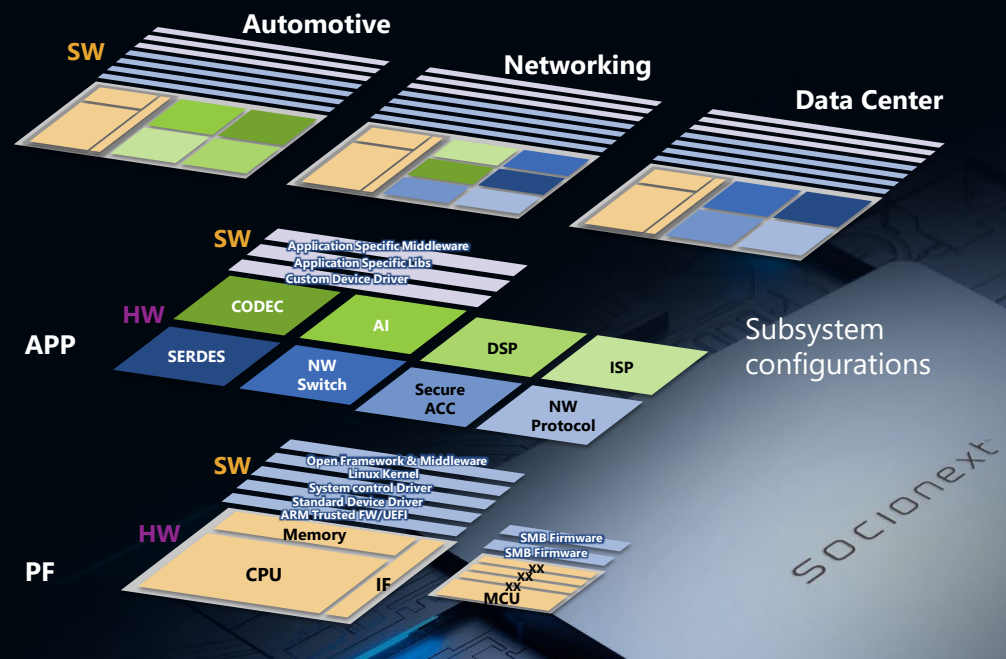
- Software-Defined SoC
  - as part of a software-oriented system
- Requirements
  - Computer architecture basis
    - High-performance computing
    - Standard software
  - Application specific parts
    - High-speed interface
    - Hardware accelerator
    - Chiplet
    - …
  - Integration with software

Expanding to automotive chiplets

- To add automotive requirements to the common platform
  ›› Platformization / Standardization

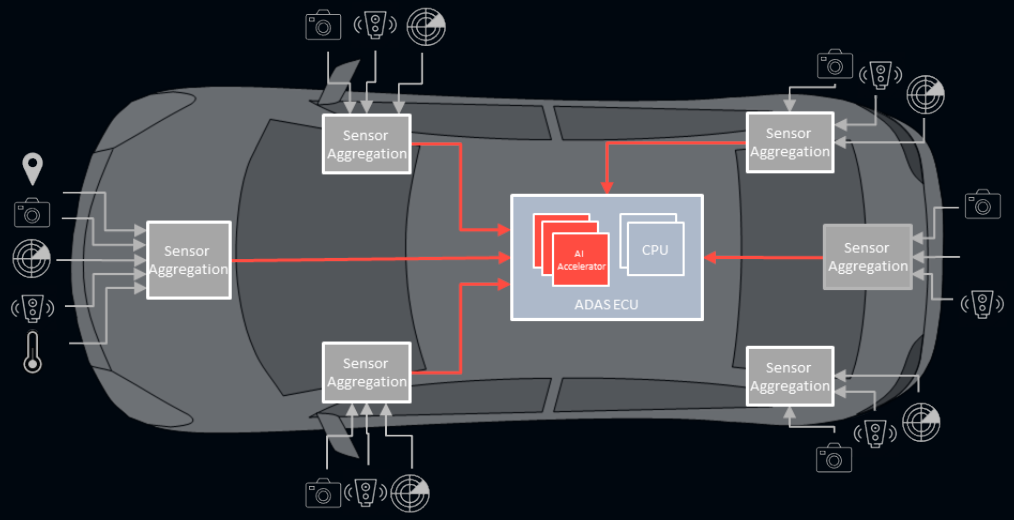
- To strengthen the relationship with ecosystem partners, including EDA, IP, package, fab, and others, thus enabling global innovation to better manage solution and system’s life cycle

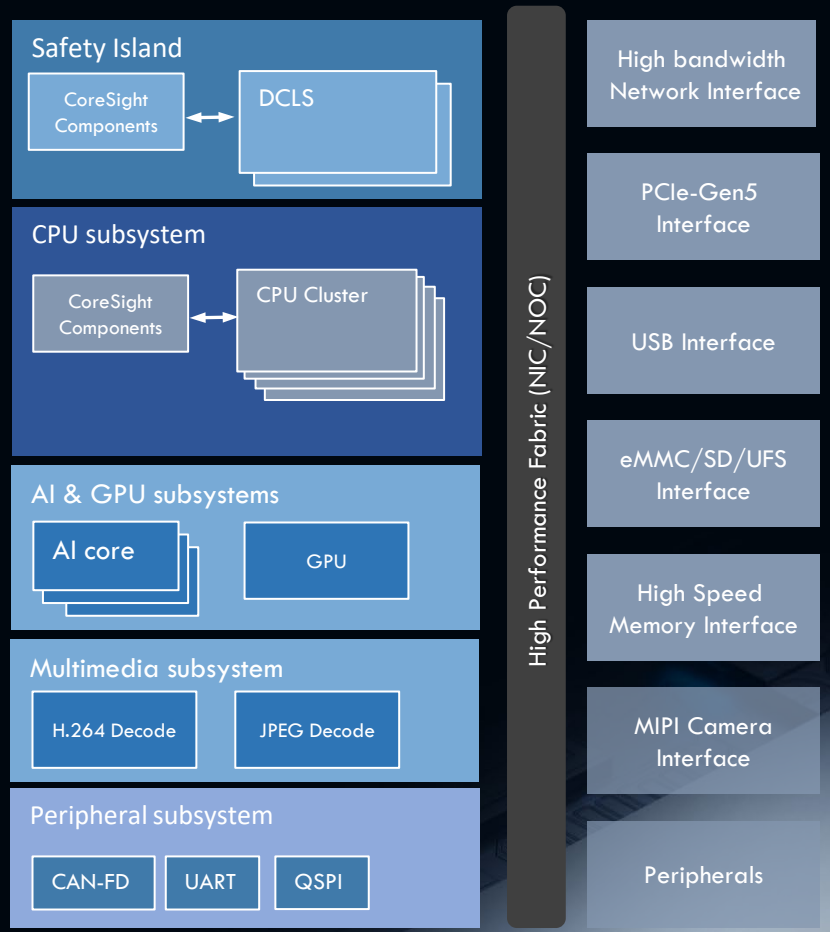




Key Components for Automotive SoC for ADAS and Central Compute (HPC) Applications

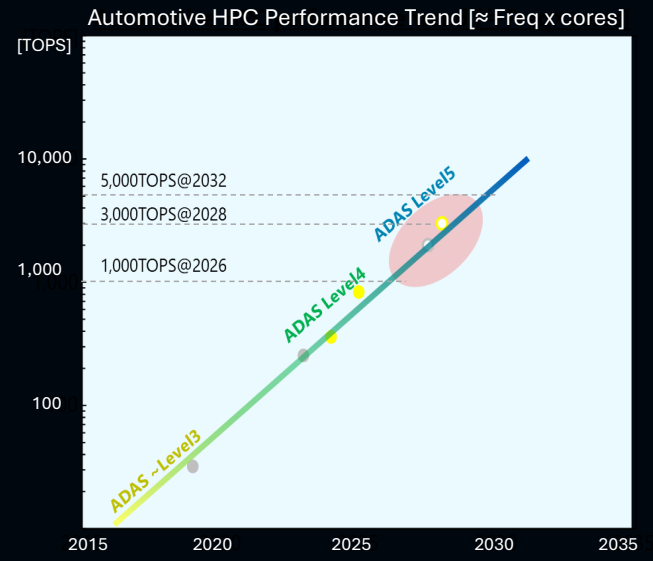
- Leading-edge process development @ 5nm, 3nm, and 2nm
- Large die size, with increased memory density for AI and GPU
- Specialized IP (hardware/software) for AI acceleration
- High-speed network, memory, and host interfaces
- Complex CPU subsystem and NOC interconnect
- Image processing and DSP
- High-performance advanced packaging, including MCM and chiplet
- ISO26262 development flow for ASIL-B/C/D
- Automotive qualification of each IP/chip and the whole package

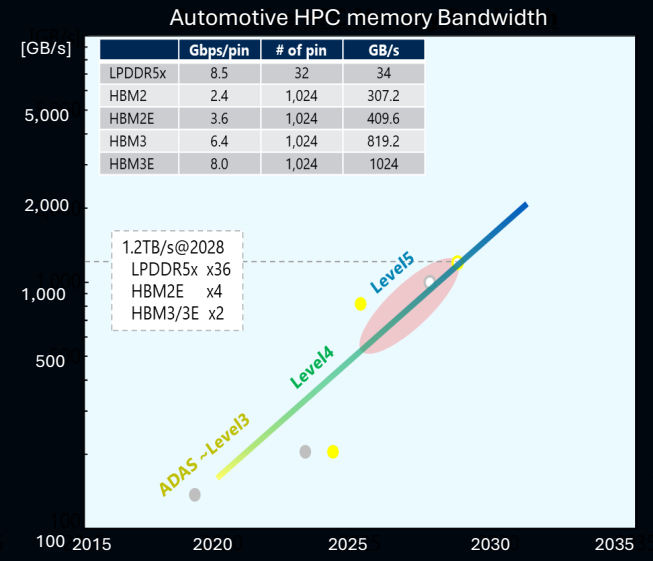




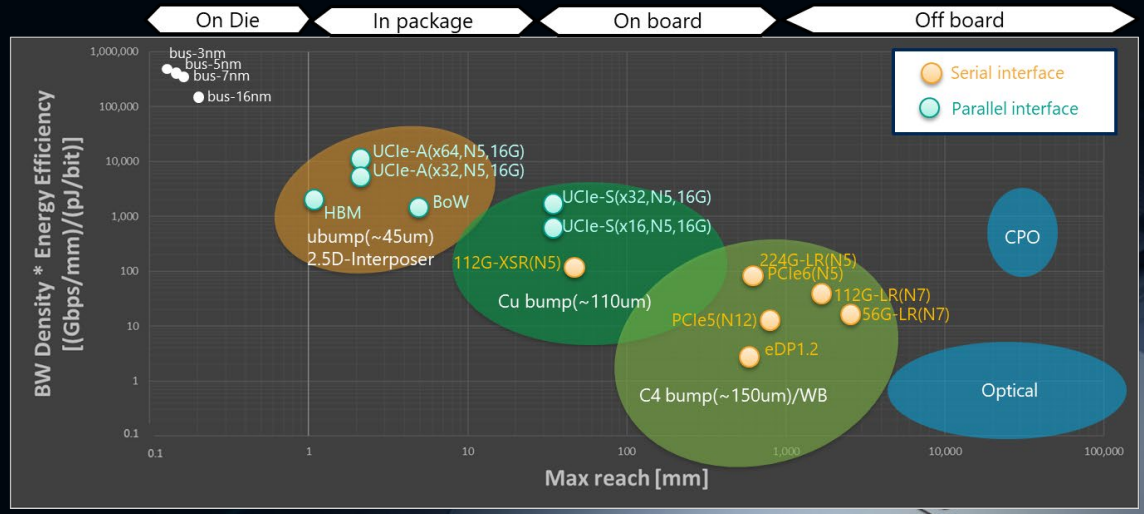
Automotive System Requirements Leading to Disaggregation

- HPC 〉〉Chiplets ＋ HBM/LPDDR5x + UCIe
  - High speed data processing via highly integrated multi-core compute, dedicated DSP & AI engines enabling up to ADAS level 5
  - Memory Bandwidth reaching to 300GB/s and 500GB/s (HBM*E) for level 4 and 5, respectively
  - High performance/high bandwidth, distributed across chiplets is required to achieve the necessary TOPS for ADAS level 3-5
- Automotive LSI 〉〉Quality assurance involving chiplet
  - High quality and reliability - guaranteeing operation in an automotive environment will be required
  - Foundry/OSAT certification for mass production of chiplet based designs is on-going





	Gbps/pin	# of pin	GB/s
LPDDR5x	8.5	32	34
HBM2	2.4	1,024	307.2
HBM2E	3.6	1,024	409.6
HBM3	6.4	1,024	819.2
HBM3E	8.0	1,024	1024



What is Driving Chiplet Strategy?

- Semiconductor development schedule, cost, and performance are significant issues leading to the creation of chiplets
  - The gap between required chip performance and IO performance evolution
  - Increase in die and development costs due to miniaturization

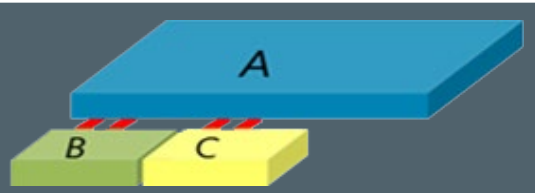
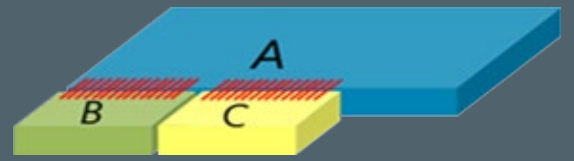
Application Requirements	Traditional Approach	Issues	Chiplet Value-Add

Higher performance	▪ Advanced process node	▪ Mask/die cost ↑
		▪ Yield issues
			▪ Split die's Homogenous
			▪ Split die's Heterogenous
			  ▪ Optimal process selection per die
			  ▪ Functional split die's
			▪ Smaller die
			  ▪ Better yield
			  ▪ Faster development and qual
			  ▪ Lower cost
			▪ Challenge moving to package development
			  ▪ More flexibility

	▪ Dedicated HW ▪ More CPU/GPU/AI accel ▪ More memory/$'s	▪ Die size limit	
Variability and extensibility of product	▪ Re-design/manufacture entire chip	▪ Development/Qual cost ↑ ▪ Time to Market	▪ Partial HW update/evolution ▪ Time to market advantage due to limited changes
Partial upgrade plan			
Low power Connect power on PCB		▪ PCB implementation difficulty	▪ Small FP and fine pitch of Chiplet ▪ Low power/High BW connection

Are Chiplets Superior to Monolithic SoC/SiP ?

- Chiplets enable the same silicon design to be deployed in many system-level solutions
  - Achieve performance better than monolithic SoC by applying low-power, low-latency dedicated Interfaces such as UCIe
- Chiplets enable new ways to focus on customer's investments
  - Solves issues of time-to-market associated with leading Si process nodes
- Enabling Technology: packaging technology innovations are helping to drive economies of scale

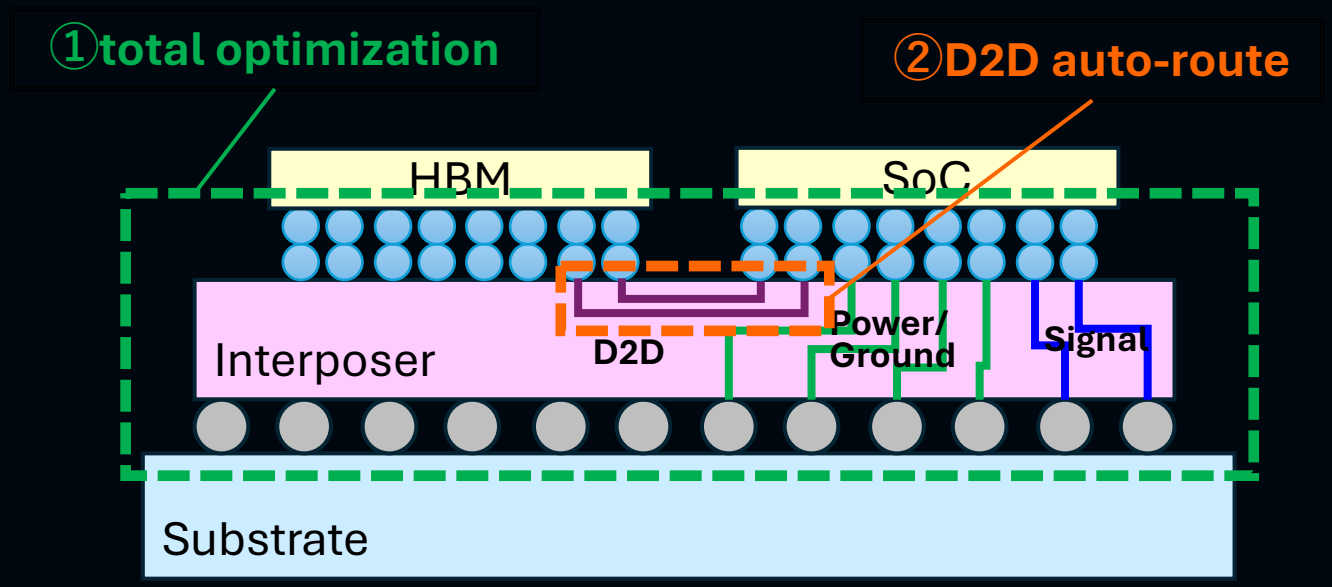
	Conventional SiP	Chiplets
Structure		
IF between chips	Conventional IF	Specified IF with low power and low latency
Interconnect technology	Wire or Bump interconnectivity on the conventional package substrate	Wide base parallel interconnectivity with fine pitch interposer and TSV-3D stack - or - High-speed serial interconnectivity on conventional package substrate
Performance	≤ Monolithic SoC * Lower power efficiency and higher latency	≥ Monolithic SoC * To compensate for SiP drawbacks with specified IF; enable lower-cost solutions

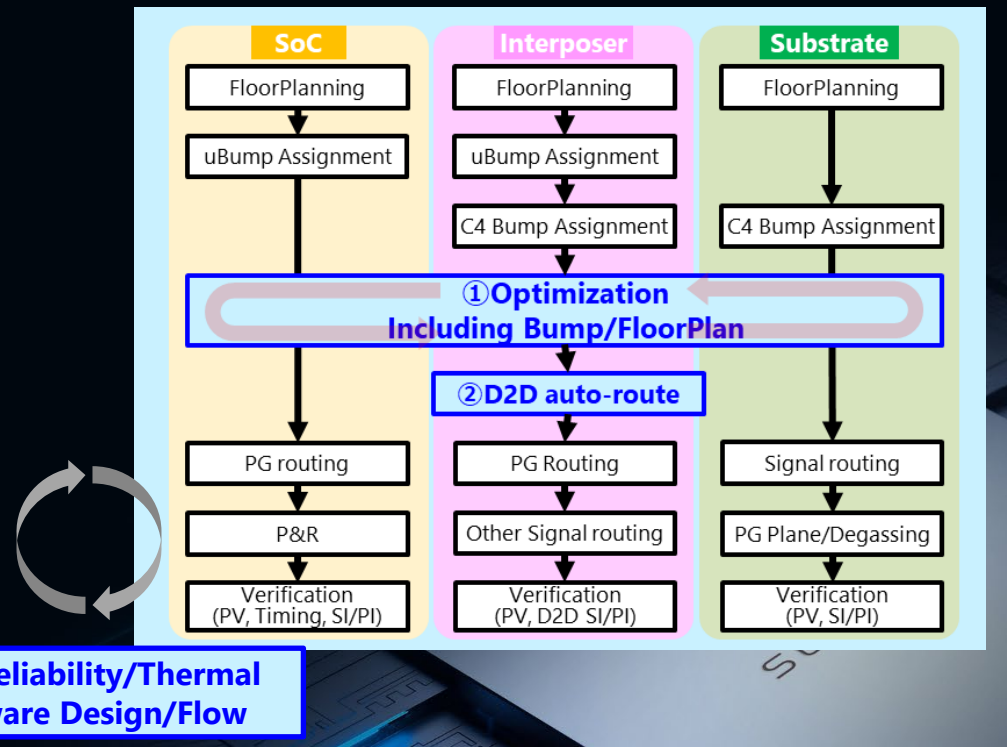
SiP: System in Package

Design Challenges for 2.5D/3D Chiplet SoCs

Challenges

- Design optimization to achieve maximum performance considering SoC/Interposer/Substrate interaction
- Continuous update of design rules and interaction between Chiplet/Interposer/Substrate need to be automotive grade ›› automated design is mandatory
- Reliability and thermal aware design for stable, low power package with better PI/SI
- Flexible combination of 2.5D/3D, RDL/Si and D2D as chiplet components

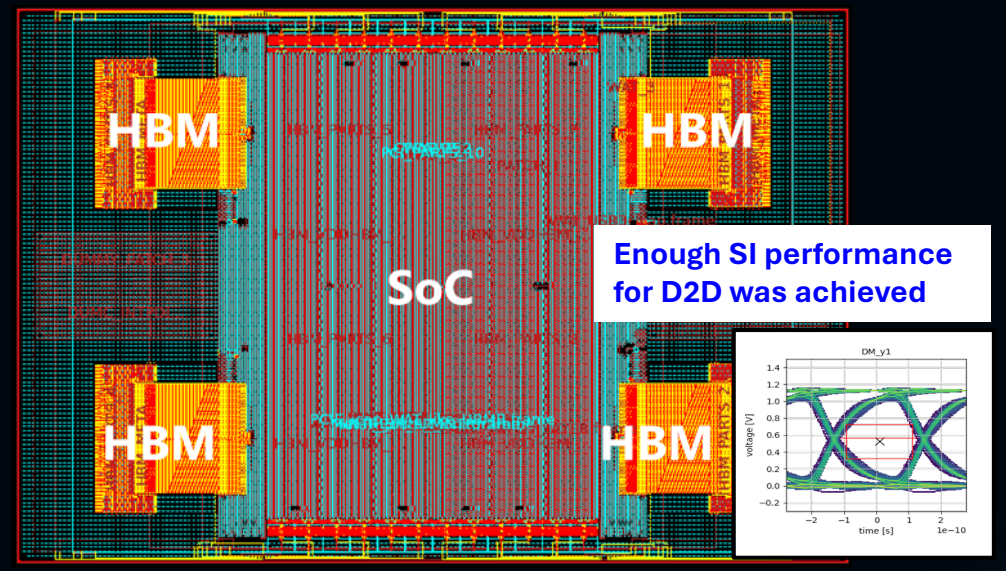




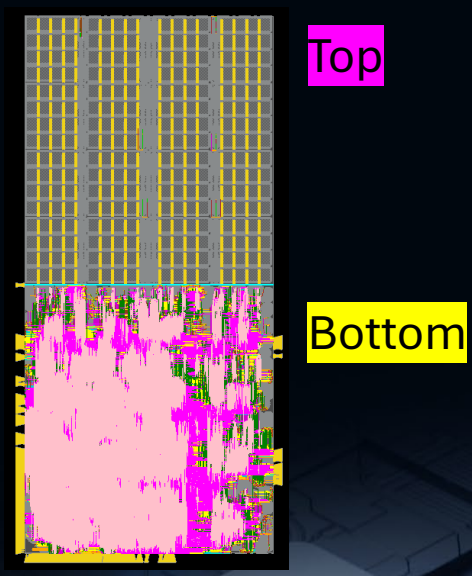
Flexible and Robust Design Provides Time-to-Market Advantage

Socionext Initiatives in practical SoC design

- Established an automated design environment of 2.5D/3D Chiplet with eco-system partners
- Reliability/thermal aware design/verification environment has been built in collaboration with IMEC and eco-system partners with automotive robustness



Optimization with auto-routing and designed view with HBM(2.5D chiplet)



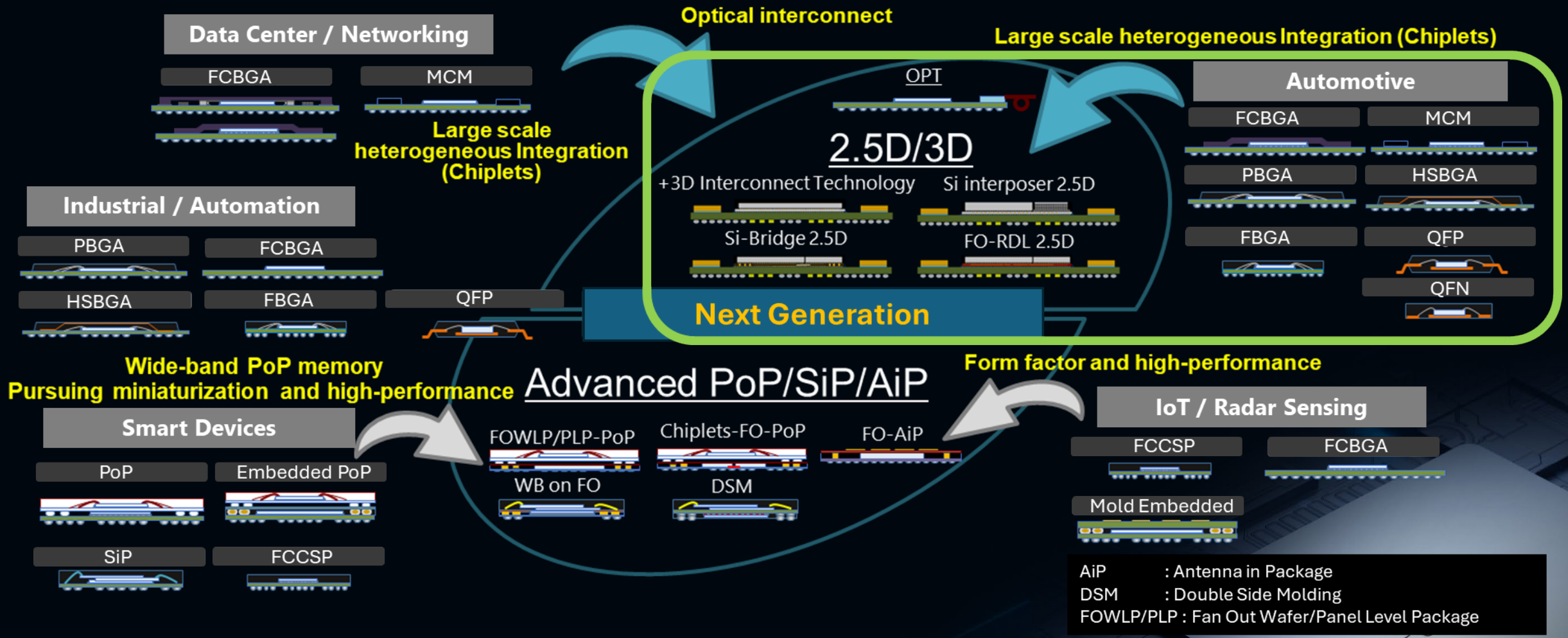
Designed view of 3D chiplet

Flexible and robust design flow/validation for various component combinations

➔Need design/validation standardization through ACA/APC activities

Packaging Technologies

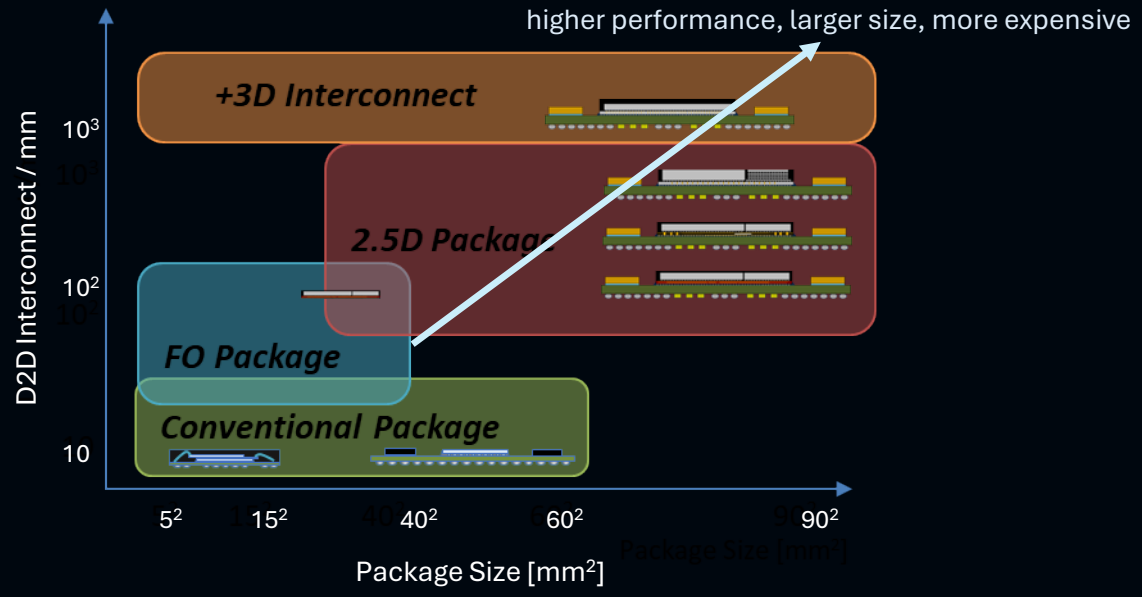
- Performance requirements driving the ADAS shift to larger chiplet solutions



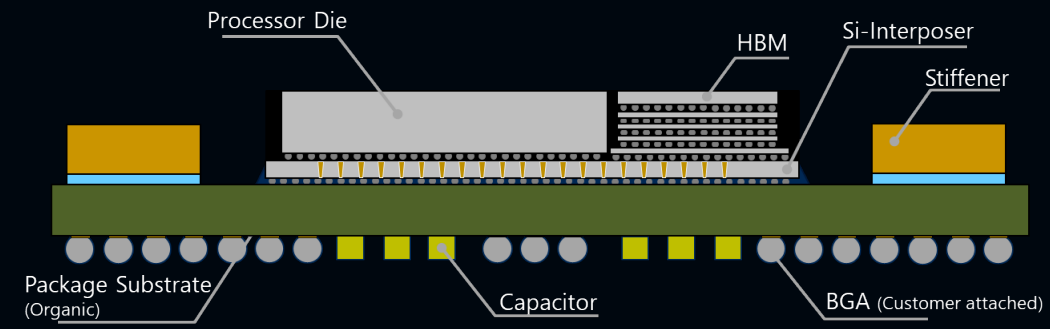
Fabrication Challenges for 2.5D/3D Chiplet SoCs

Challenges

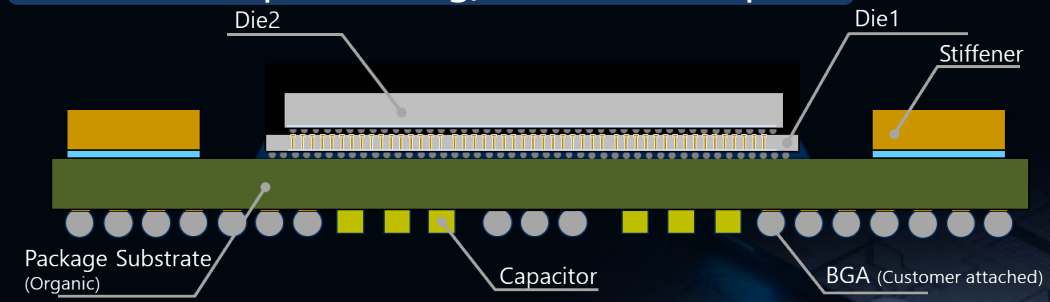
- Large Die and interposer size
- Stable fabrication across multi-physics of **electrical, thermal and mechanical**
- Consideration of new elements (components, materials, structure) and failure modes
  ›› Nanosheet, CFET, backside-PDN, interposer, hybrid-bonding, integrated capacitor and so on.
- Testing solution enabling parallel tests of all die and D2D testing



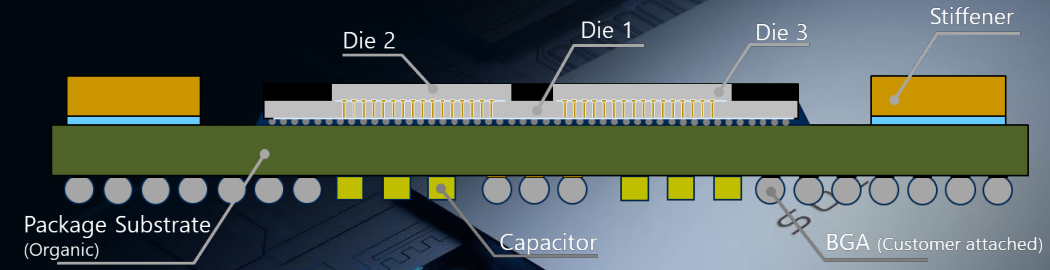
Si Interposer 2.5D Chiplet



Micro-bump Bonding/TSV 3D Chiplet



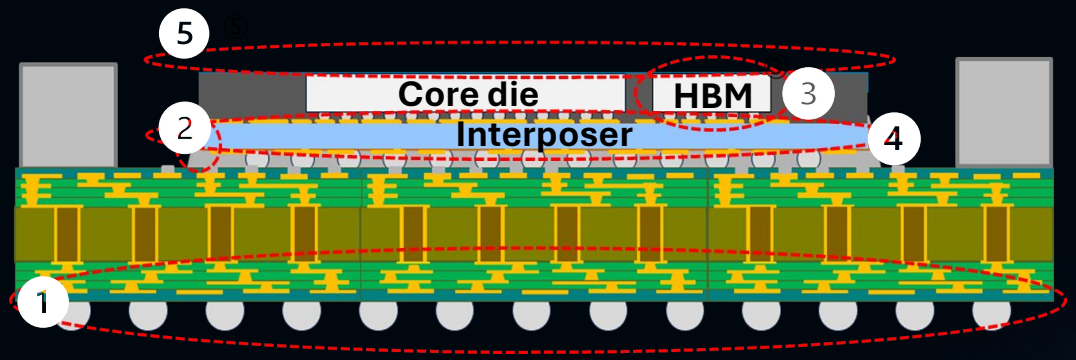
Hybrid Bonding 3D Chiplet



Fabrication Challenges with Large Chiplets

Potential issues for fabrication

1. Coplanarity / thermal warpage of large package body size
   ›› Material selection, structural design rule,...
2. Large interposer module assembly and structural reliability
   ›› Interposer type selection, material selection, structural design rule,...
3. HBM's physical compatibility with RDL/Si interposer structure
   ›› Structural design rule, material selection,...
4. Interposer
   ›› Routing design rule, capacitor option,...
5. Thermal management
   ›› Top surface flatness, TIM1 lineup,...



Overcome Difficulties

Socionext Initiatives in practical SoC design

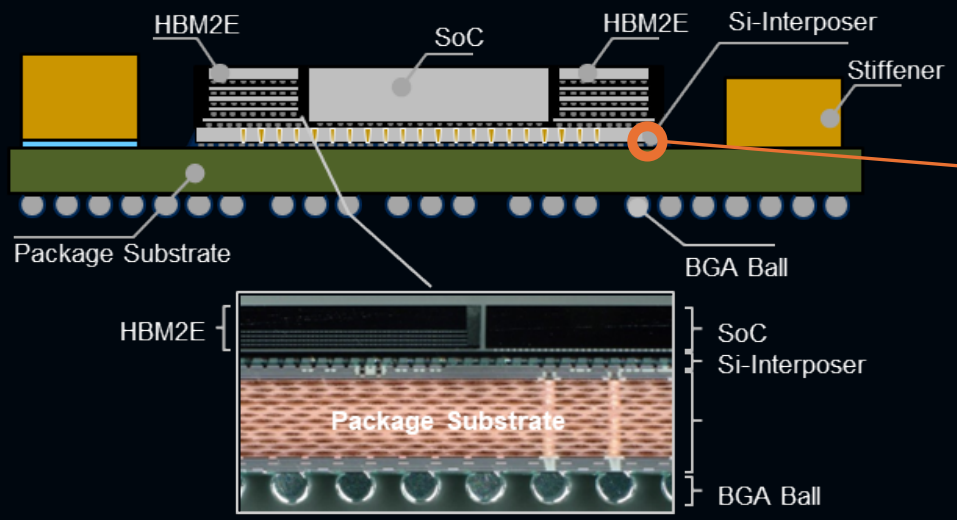
- Learning with own TVs (Test Vehicles) and validating automotive qualification

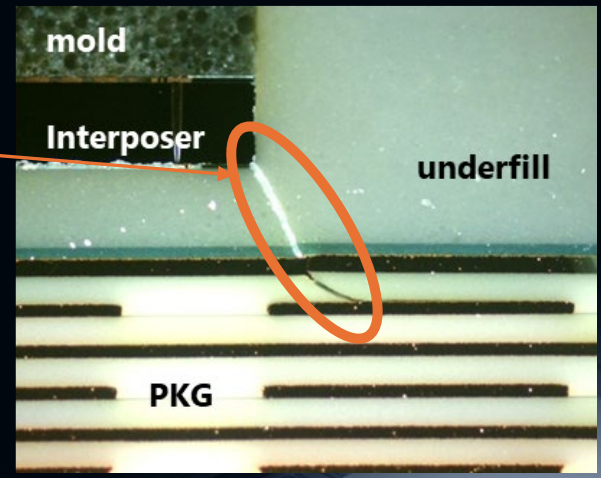
- Scenario -

A crack mode in the underfill region occurred due to the thermal expansion difference between the large-scale interposer and PKG

〉〉 Feedback to design

〉〉 Change the floor plan of a package





The quality and reliability of large chiplets are essential for mass production of automotive

➔Need for standardization of QnR and AEC-Q through ACA/ACP activities

Aiming for ZERO Defects

- Continuous cycle with design, methodology, eco-system, and standardization
- Quality assurance enables safe and secure automotive operation and applications

Functional Safety (ISO26262)

- AFSP Qualified Engineers
- Development Process
- Safety Mechanism
- ASIL-B/C/D

Test Strategy

- Reinforced test
- Screening test
- Stress test

Failure Response

- Failure Analysis
- Response Time
- Improvements
- Monitoring Silicon Lifetime
- Redundancy

Design Strategy

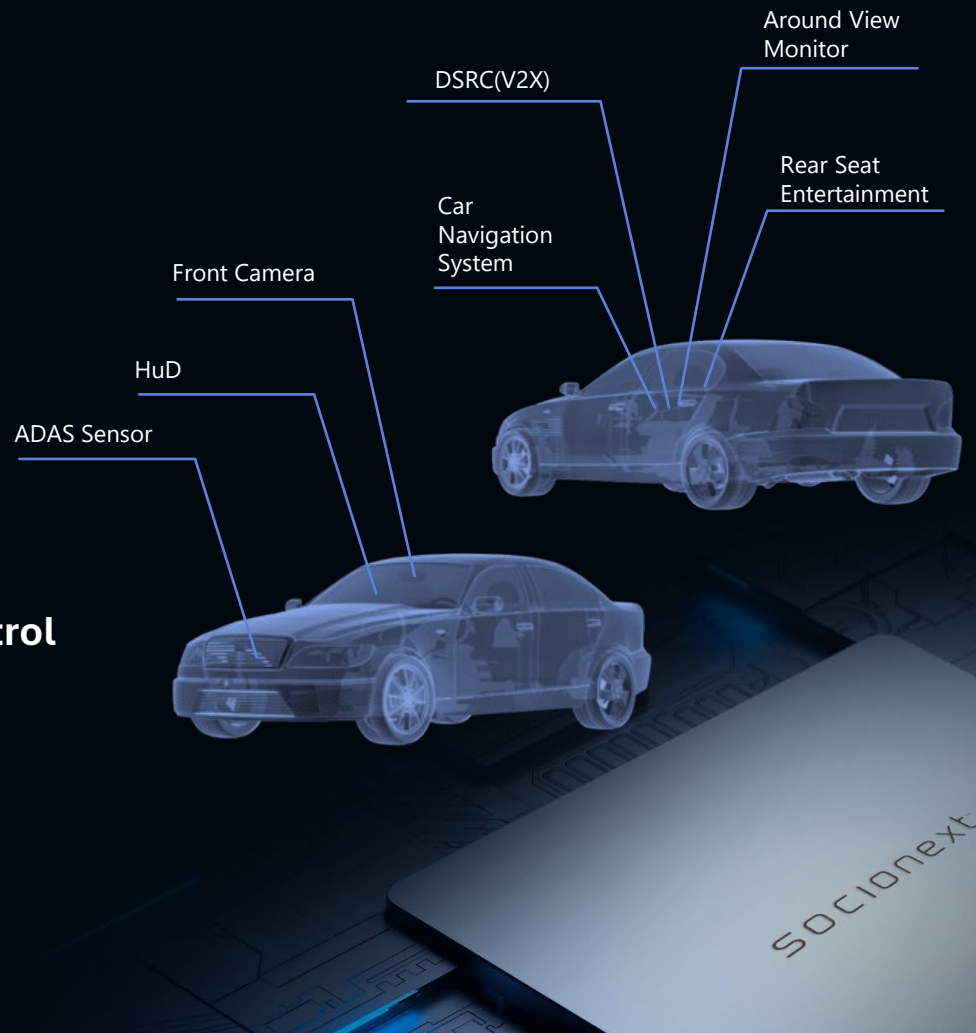
- High coverage DFT
- Automotive DFM
- Automated Chiplet Design Flow

Reliability Test & Documentation

- IATF16949
- AEC-Q100/104
- PPAP

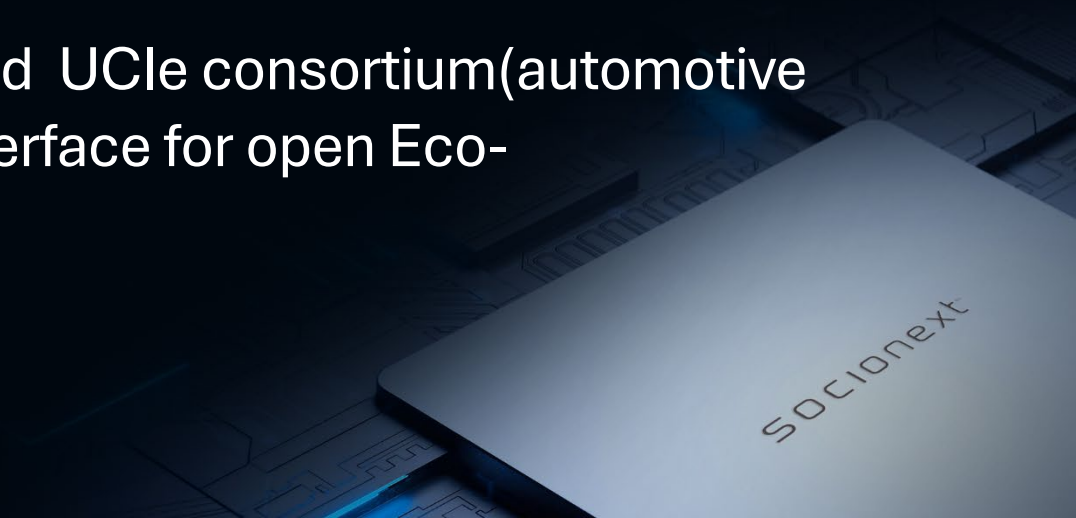
Production Process Control

- Wafer Process
- Assembly
- Test



Call to Action

- Build the standard design process/functional safety/AECQ flow for automotive with chiplet to accelerate time-to-market
- Explore 2.5D/3D Chiplet failure modes for standardization of qualification including chiplet + w/ and wo HBM
- Enhance collaboration with foundries to expedite completion of qualification for 2.5D/3D chiplets
- Establish a tighter relationship between ACA and UCIe consortium(automotive working group) to strengthen the high-speed interface for open Eco-System/Chiplet

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